J. Indian Inst. Sci., 65(A), Oct. 1984, pp. 129-142

A new companding DAC for PCM telephone codecs

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Abstract

This paper presents a new architecture for companding DAC required in PCM telephone codecs and suitable for IC realization. This DAC has facilities for pin-selecting μ/A laws, use in encoder/decoder operations and with unipolar/bipolar V_{ref}. An approach to optimizing this DAC using CAD techniques is also covered here.

Key words: Companding DAC, PCM telephone codecs.

1. Introduction

The companding DAC is an important building block of PCM telephone codecs. Such a DAC is generally characterized by μ-law or A-law transfer functions. With the advent of IC technology PCM speech codecs in single-chip IC form have become popular. For realizing improved performance of such a codec, it is now preferable to incorporate the following features into the companding DAC.

(i) Facility to pin-select μ / A laws
(ii) Use of one companding DAC per PCM speech codec
(iii) Use of minimum reference voltage sources
(iv) Simple circuit arrangement
(v) High speed of conversion

These requirements are brought together in developing a new architecture for the companding DAC. This is described here together with its analysis and design optimization using computer-aided design (CAD). By employing CMOS FETs for this realization, it is expected that the companding DAC will facilitate high performance of the PCM codec.

2. The new companding DAC

The following two alternative methods were considered to realize the companding DAC characteristics given above. Figure 1 gives these two methods in block schematic form. Figure 1(a) uses one reference voltage ($+V_{ref}$) source and fig. 1(b) uses two reference voltages ($\pm V_{ref}$) for the entire companding DAC.

As shown in fig. 1, D1 through D8 constitute the PCM input to the companding DAC. The MSB D8 is used as a sign bit, which controls positive/negative polarity of the transfer characteristics by means of the polarity control circuit (PCC). The next MSBs (D5-D7) are segment bits, which generate segment levels by employing segment-voltage generator (SVG). The LSBs (D1-D4) are step-size bits, which are required to provide 16 equal steps within each segment level, by using step-size voltage generator (SSVG). The switch driver circuits

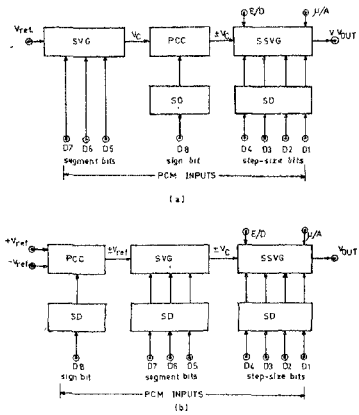


FIG. 1. Schematic block diagrams of companding DAC using

a. One reference voltage $+V_{ref}$.

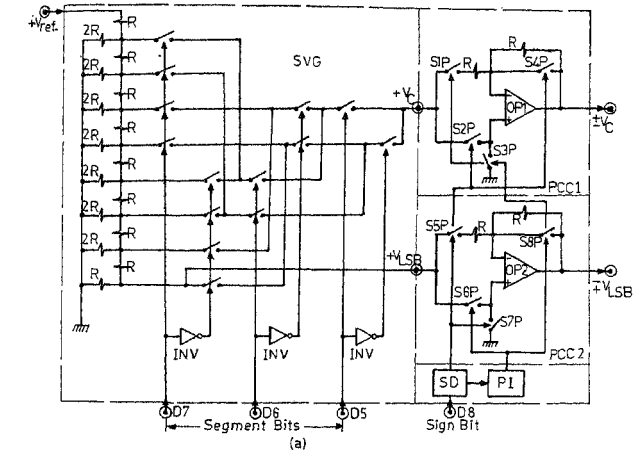
b. Two reference voltages $+V_{ref}$ and $-V_{ref}$.

(SD) establish ± voltage control to drive the analog switches (ASWs) of SVG, SSVG and PCC. The output of the SSVG is indeed the companding DAC output voltage (V_{out}), which also provides pin-selectable μ/A-law characteristics for encoder/decoder realization. The detailed block diagrams of the new companding DAC are described below.

(i) Segment voltage generator (SVG)

The following two alternative methods can be considered for generating segment voltage levels with both the polarities of the μ/A-laws companding DAC:

(a) Single reference voltage source (μ V_{ref}): The segment-voltage generator (SVG) connected with polarity control circuits (PCC) of the segment levels generator is shown in fig. 2(a). This uses $+V_{ref}$ source to the input node of SVG. The SVG uses R-2R ladder network together with a switching matrix and inverter circuits (INV). The SVG output is $+V_C$ ($=N.2^C$), where c is the segment number 0-7, which can have eight levels controlled by segment bits D5-D7, and N is V_{LSB} ($=V_{ref}/2^8$). The resulting $+V_C$ is applied to the PCC1, which is implemented by the operational amplifier OP1 and the analog switches (ASWs) S1P-S4P, which are driven by MSB D8, followed by a switch driver (SD) and polarity inverter (PI) circuits. Hence, the output from this circuit under the control of D8 is $\pm V_C$. The $\mp V_{LSB}$ is obtained from the LSB node of SVG followed by the PCC2 (OP2 with the ASWs S5P-S8P) under the control of D8 followed by SD and PI circuits and keeps it out of phase



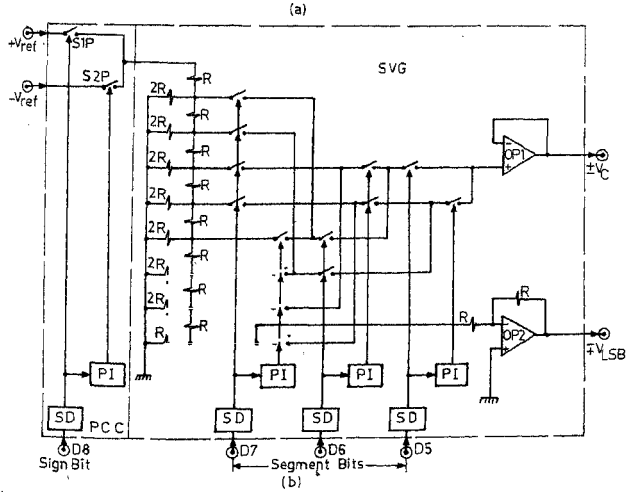


FIG. 2. Segment voltage generator for the new companding DAC.
a. $+V_{ref}$ scheme. b. $\pm V_{ref}$ scheme.

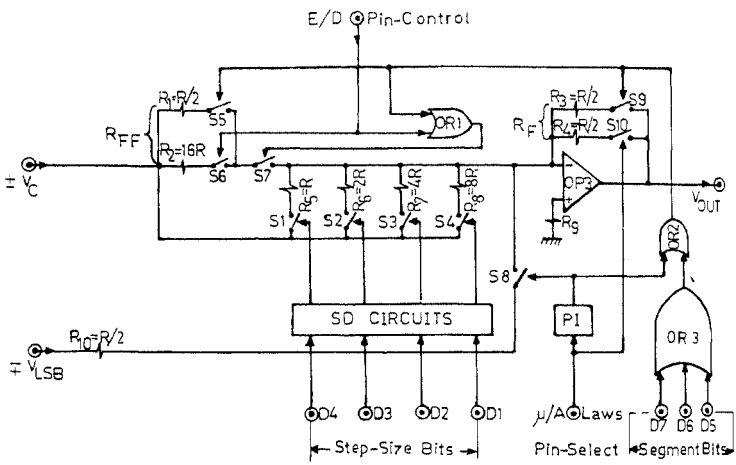


FIG. 3. SSVG of the new companding DAC.

w.r.t. $\pm V_C$. This voltage helps to obtain the μ-law characteristic through the operation of ASW S8 (as shown in fig. 3) which is discussed in a later section.

(b) Bipolar reference voltage sources ($\pm V_{ref}$): A detailed block diagram of segment level generator with both the polarities using $\pm V_{ref}$ sources is shown in fig. 2(b). The $\pm V_{ref}$ sources are transferred to the input node of SVG (using R-2R ladder network together with a switching matrix, SD and P1 circuits followed by a buffer amplifier OP1) through the PCC. This is implemented by the ASWs S1P-S2P, which are, in turn, controlled by D8, followed by SD and P1 circuits. Hence the output of SVG has both the polarities, *i.e.*, $\pm V_C$. The $\mp V_{LSB}$ is obtained from the LSB node of SVG followed by unity-gain inverter OP2, which keeps it out of phase w.r.t. $\pm V_C$ similar to that in fig. 1(a)

(ii) Step-size voltage generator [SSVG]: The SSVG (fig. 3) uses the binarily-related resistor quad (R, 2R, 4R, 8R). The inputs to the SSVG are $\pm V_C$ and $\mp L_{SB}$ from the SVG. The ASWs S1-S4 are controlled by the step-size bits D1-D4, followed by the SD circuits. The SSVG is provided with controls for selecting μ/A-laws and encoder/decoder (E/D) operation through pin-select terminals. The ASWs S5-S10 together with resistors R_F and R_{FF}, and OR-gates OR 1-OR 3 facilitate this (Table 1). Hence, the output voltage V_{OUT} of this circuit is the output of the μ/A-law companding DAC.

Table I
Operation mode of step-size voltage generator (SSVG)

Condition	μ/A-law pin-select	E/D pin-control	Operation of analog swtiches						Law	Operation mode
			S5	S6	S7	S8	S9	S10		
I	Low	Low	ON	OFF	ON	ON	ON	OFF	μ	DECODER
II	Low	High	ON	ON	ON	ON	ON	OFF	μ	ENCODER
III	High	High	*	ON	ON	OFF	*	ON	A	DECODER
IV	High	Low	*	OFF	*	OFF	*	ON	A	ENCODER

* The analog switches S5, S7 and S9 work under the control of segment bits D5-D7.

3. Design optimization

The design optimization of the new companding DAC circuits is carried out using CAD and SPICE-2G simulation program. In this, analog and digital circuits of this DAC have been combined using the same model parameters of CMOS FETs (Table II) which have be taken from published literature[1]. These parameters are helpful in the realization of PCM codec using this new DAC as a single-chip IC. The device dimensions of CMOS FETs *viz.*, channel length, L, and channel width, W, are given in μm, and the ratios shown in the following figures are W/L. The resistor networks used here are assumed to have close tolerance in R values, consistent with current monolithic IC technology and this is acceptable in the design.

(i) Operational amplifier (OP AMP)

Figure 4 gives a typical circuit schematic of the CMOS OP AMP presently used in telecommunication applications[1] with very low input offset voltage. It consists of two gain stages with a total gain of about 60 dB. A buffer stage is used in the feedback compensation loop to eliminate an understandable zero at g_m / C_c. The OP AMP has a useful feature associated with

Table II
CMOS FETs model parameters

Parameters		Values	
General	SPICE-2G	Driver	Load
		n-channel	p-channel
V_T (volt)	VTO	1	1
N_B (cm^{-3})	NSUB	5×10^{15}	1.5×10^{15}
μ_0 (cm^2/vs)	UO	600	300
X_j (μ_m)	XJ	2.2	1.2

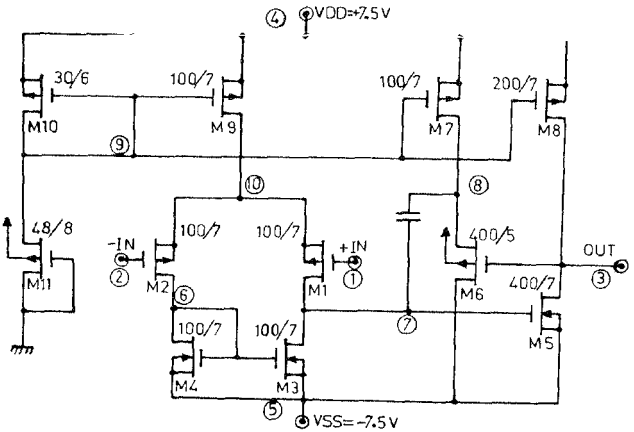
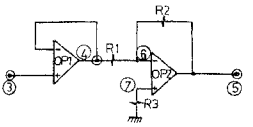


FIG. 4. Circuit schematic of CMOS OP AMP

the fact that all transistor channel lengths L_s are nearly equal, which guarantees equal V_T for all the transistors. The values of W and L of all MOS FETs of this OP AMP are chosen following Wong and Salama[1] and the same are shown in fig 4. The DC, AC and transient analysis of this OP AMP are simulated for inverter and non-inverter operations. Important results of this design are given in fig. 5 and Table III.

Table III
Results of design: Analog/Digital blocks

Parameters	Values				
	OP AMP	SD	ASW	PI	PR-Gate
Power supply (volt)	± 7.5	± 7.5	± 7.5	± 7.5	± 7.5
Power dissipation (watt)	60.8×10^{-3}	2.65×10^{-3}	—	3.12×10^{-10}	9.36×10^{-10}
Number of devices used	12	7	1	2	6
Operating speed (MHz)	—	> 1	> 1	> 1	> 1
Band-width (– 3dB)	3.9 MHz	—	—	—	—
Output linearity range (Volt)	+ 6.545 to −6.074	—	—	—	—
R_{ON} (ohm)	—	—	≃ 80	—	—
R_{OFF} (ohm)	—	—	≃ 10^{10}	—	—



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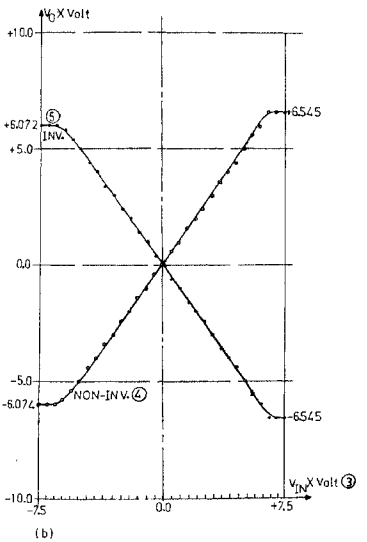

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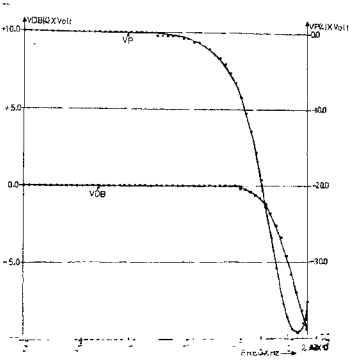

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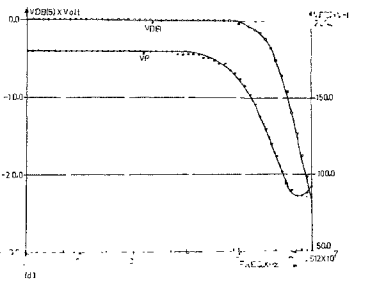

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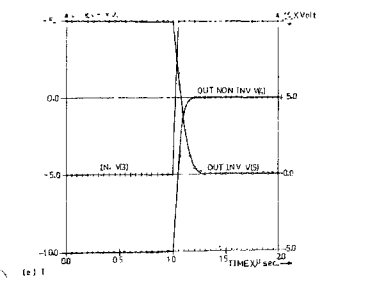


(e)

FIG. 5. CMOS OPAMP design characteristics.

a. Non-inverting and inverting operations.

b. DC transfer characteristics.

c. AC analysis of non-inverting configuration.

d. AC analysis of inverting configuration.

e. Transient analysis of inverting and non-inverting configurations.

(ii) Switch driver circuit

This circuit is required at different stages of the companding DAC to drive the various ASWs. Such switches require to be driven by signals of either positive or positive-and-negative voltage levels. These are produced from a digital input which is usually positive logic by employing SD circuits. Figure 6 gives the SD circuit using CMOS FET devices. In this, positive logic input (V_H = logic '1') is applied to the non-inverting (+) terminal of the differential amplifier, which uses a fixed bias. This bias circuit *i.e.,* M1 and M2 can be used to drive all CMOS FETs in the SD circuits required for the entire DAC. As can be seen here, the output of the SD circuit is,

$$V_0 = -(V_{in} - V_{Bias})\, A_d \tag{1}$$

where, A_d is the gain of differential amplifier, V_{Bias} can be chosen equal to $V_H/2$ by appropriate dimensional (i.e., W and L) control of $M1$ and $M2$, and V_{in} assumes '0' (0 volt) or '1' (V_H). The dimensions of $M3-M7$ are chosen to realize appropriate A_d which decides the output voltage levels of the circuit. In order to test the effectiveness of this SD, an ASW is also simulated. In this, $W = 40\ \mu m$, $L = 0.5\ \mu m$ and n-channel type are considered satisfactory for ASW to yield low R_{ON} and high R_{OFF}, following Crawford[2]. Results of this design are given in fig. 6(b) for the SD circuit together with ASW. As can be seen from this figure, the output of the SD circuit is applied to the ASW so as to facilitate the transmission of the analog signal *i.e.,* a sine wave with 1 MHz frequency and ± 5 volt peak-to-peak amplitude. The results of transient analysis of this circuit are computed and given in Table III.

(iii) Digital circuits

The μ/A-law transfer characteristics, μ/A-law pin-selectable operation and E/D operation mode of the new companding DAC are controlled by the digital circuits PI, and the OR-gates. The values of $W = 14\ \mu m$ and $L = 7\ \mu m$ for p-channel, $W = 7\ \mu m$ and $L = 7\ \mu m$ for n-channel are chosen for all the MOS FETs of these circuits. Figure 7(a) gives a typical circuit for the CMOS FETs PI circuit. The DC analysis and transient analysis of this design are shown in figs. 7(b) and (c) respectively. Also, fig. 8 gives a circuit diagram and the results of transient analysis of the two input OR-gate. The important results of these analyses are also summarized in Table III.

(iv) The new CMOS companding DAC

The following two design steps were finally arrived at as a result of the optimization technique using CAD for the new companding DAC circuit:

(a) Design step I: The μ-law and A-law transfer characteristics of the companding DAC have 15 and 13 segments respectively in both the polarities. In this design, it was found adequate to achieve the realization of these characteristics at the first two positive segments closest to the origin as the same can be easily extended further.

The SSVG shown in fig. 3 is simplified by omitting the SD circuits and OR-gate OR3. Then D5 is applied to the input terminal of the OR-gate OR2 which is used for realization of A-law characteristics. The resistors used in this circuit relative to R are calculated from the theoretical analysis of this DAC indicated in Salem and Sonde[3]. Resistor R equal to 5 K ohm

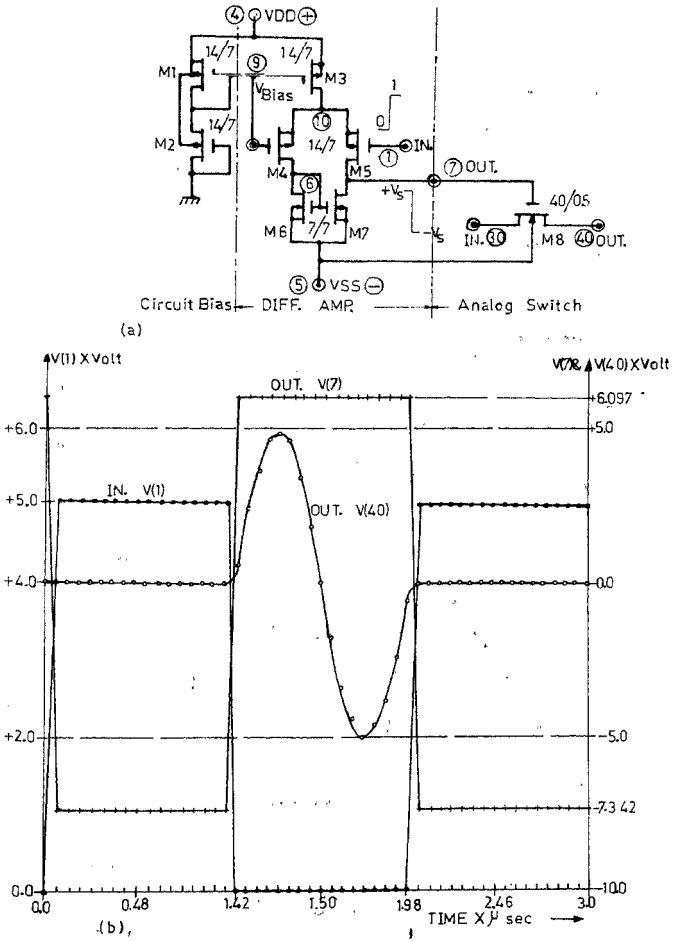
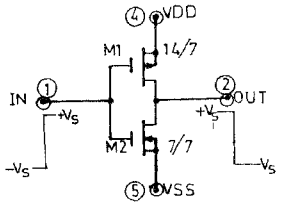


FIG. 6. SD and ASW design characteristics. a. Circuit diagram. b. Transient analysis.



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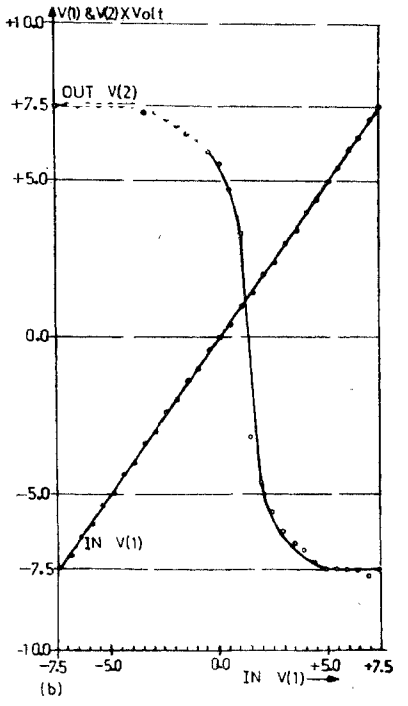

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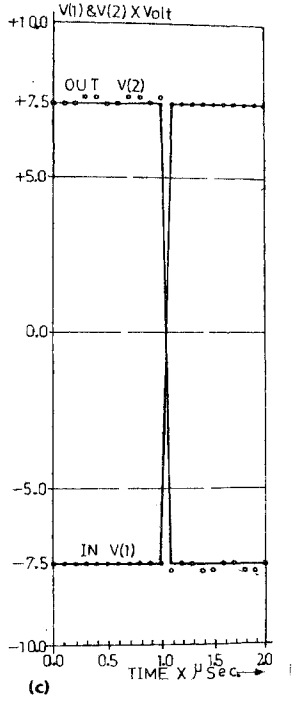

(c)

FIG. 7. PI design and characteristics.

a. Circuit diagram.

b. DC analysis.

c. Transient analysis.

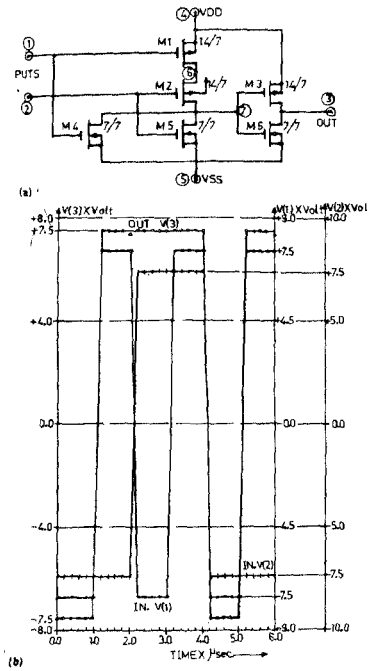

FIG. 8. **Two-input OR gate design and characteristics.**

a. Circuit diagram. b. Transient analysis.

was chosen for this design. The digital inputs with the DC supply voltages required for the circuit are generated by SPICE-2G simulation program. The transient analysis of this is carried out and the important results are shown in fig. 9 and Table IV.

(b) Design step II: In this design, only the positive half of μ-law characteristics and E/D operation mode are taken up for investigation as these are adequate to show the usefulness of the design procedure. Only a marginal modification is necessary to extend it to realize the A-law characteristics. Therefore, fig. 2(b) is simplified by omitting the SD circuits, unity-gain inverter OP2 and the PCC. A $V_{ref} = -5$ V is applied to the input node of the SVG. The output from SVG ($-V_C$) is used as the input to the SSVG (fig. 3). This circuit is also

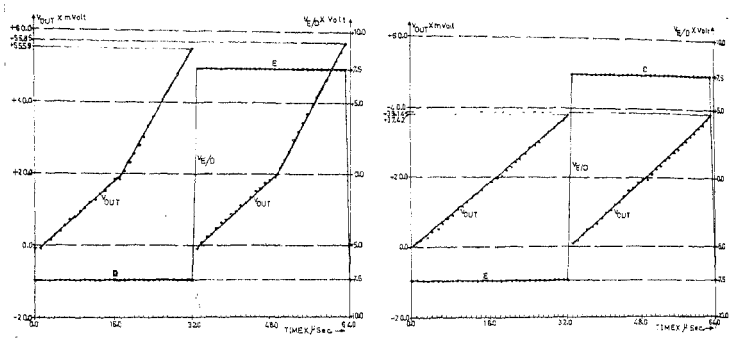

FIG. 9. Transient analysis of design step I. a. μ-Law characteristics. b. A-Law characteristics.

simplified by omitting active/passive devices required for A-law characteristics (OR-gates OR 1-OR3, PI, ASWs S5 and S7-S10, and resistor R4) and SD circuits. The resistor values used in the ladder network of SVG were chosen equal to 10K ohm and 20 K ohm, whereas the resistor R of the SSVG was chosen equal to 5 K ohm in this design. Other resistors relative to R are also computed as indicated in Salem and Sonde[3]. The digital inputs, DC voltage and V_{LSB} required are generated by SPICE-2G simulation program. The results of transient analysis of this design are also computed and the important results are shown in fig. 10 and Table IV.

Table IV
Results of design steps I and II

Parameters			Values	
			Design step I	Design step II
Supply voltages (volt)			± 7.5	± 7.5
Reference voltage V_{ref} (volt)			−5	−5
Power dissipation (m watt)			74	140
Time of conversion (μ sec.)			1	1
Number of active devices used			35	47
Number of passive devices used			11	26
Offset biases (m volt)	μ-law	encoder	1.14	1.215
		decoder	0.69	0.653
	A-law	encoder	0.25	—
		decoder	0.58	—
Dynamic range of μ-law (dB)		encoder	—	71.995
		decoder	—	71.91

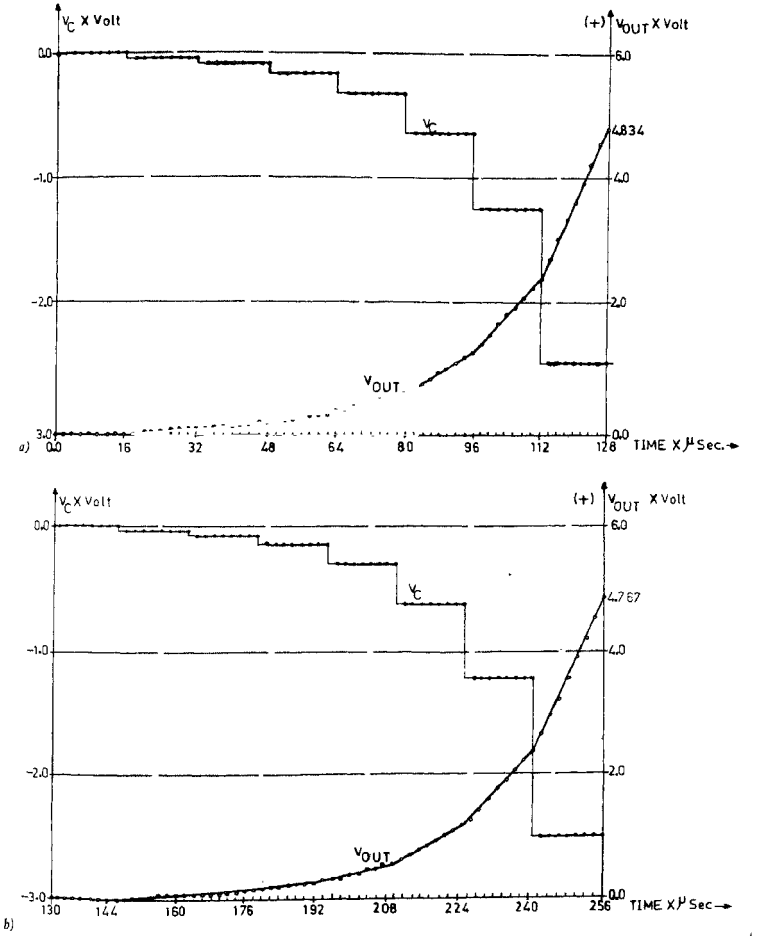

FIG. 10. Transient analysis of design step II. a. Encoder section. b. Decoder section.

4. Discussion

The circuit configuration of the new μ/A-law companding DAC required for PCM telephone codecs followed by design optimization have been presented above. The results obtained from these investigations are summarized here:

(a) A single codec circuit capable of providing either μ-law or A-law characteristics has been designed. Besides, it has been demonstrated that only one DAC need be used for both the encoder and the decoder sections of this codec.

(b) This companding DAC operates with both $+V_{ref}$ and $\pm V_{ref}$ reference voltage sources with equal ease.

(c) Offset biases of μ/A-law characteristics for the companding DAC used with the decoder and encoder sections (Mid-tread/Mid-riser biases) are controlled easily by the resistor values R_F and R_{FF} together with the OP2, OR-gates OR1-OR3 and PI circuits through the ASWs S5-S10 in the SSVG shown in fig. 3.

(d) The results obtained from the design optimization of this DAC agree with the findings of the theoretical analysis[3] in matters relating to dynamic range for encoder and decoder sections of μ-law characteristics, offset biases for encoder and decoder sections of μ-law and A-law transfer characteristics, step-size within the first two segment levels of μ/A-law characteristics, and the step-size within each segment levels of μ-law characteristics.

(e) The design has been experimentally verified[4], using ICs and discrete hardware for the different building blocks.

5. Conclusion

This work describes the development of a new companding DAC suitable for use in PCM telephone codecs. Not only is the architecture of this DAC investigated but the same has also been optimized using CAD for CMOS FET configurations.

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