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IISc THESES ABSTRACTS

Thesis Abstract (Ph.D.)

Control aspects of sub- and super-synchronous induction motor cascade with current source inverter for improved performance

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1. Introduction

The static Scherbius system having regeneration capability and high efficiency particularly in low-speed ranges is selected for analysis with a view to improve further its performance by suitable controls. Some techniques for reducing the reactive power requirement imposed by the slip-energy recovery schemes are also presented[1]. The design aspects of a current source inverter (CSI) are presented with emphasis on the selection of converter-grade thyristors, commutating capacitors and diode ratings, etc.

2. Experimental programme

The development in the field of power semiconductor devices along with large-scale integration (LSI) circuits and microprocessors (p), have made it possible to replace the dc drives by ac drive systems in many variable speed applications. The basic requirement of a converter used for controlling the speed of an induction motor is that its output voltage as well as the frequency should be variable. This requirement can be fulfilled by using either a cyclo-converter or a dc-link inverter. From the application point of view, cyclo-converter has limitations, such as circuit complexity and limited frequency range of operation. Most of the limitations are overcome by the use of dc-link inverters.

A dc-link inverter in induction motor-drive system, essentially consists of a converter, a filter and an inverter. The converter supplies a fixed or variable dc (voltage or current) to the inverter[2], an ac waveform can be synthesised from the dc, the frequency of which is decided by the switching frequency of the inverter. Such inverter is used for varying the speed of the induction motor.

3. Main results and conclusions

Many industrial variable speed-drive systems are required to operate over a wide speed range with continuous and accurate speed control. Such requirements can be easily met by a doubly fed induction motor with power electronics module placed on the rotor circuit. The arrangement employing a current-source inverter is found to be less expensive because the converter rating can be less than the motor rating. The work done for this thesis deals with the design, analysis and control aspects of a current-source inverter-fed slip-ring induction motor-drive system with

control exercised on the rotor side. By varying the rotor frequency, current magnitude, its phase with respect to the stator voltage, it is possible to cover a wide speed range. The control circuits necessary for generating thyristor gating pulses for the dual and single CSI are explained.

Development of a suitable mathematical model is necessary to evaluate the performance of the drive system[3]. This mathematical model has been used to determine the steady-state performance of the drive system[4]. Several techniques and approaches are possible to evaluate the stability performance of a drive system. In the present work eigenvalue analysis has been used to assess the stability performance of the doubly fed motor.

In variable-speed ac drives, the range of variation of power factor is important. Details of the control circuit to switch the thyristors in the power module to operate the machine are discussed. Control circuits involving the use of optocouplers and microprocessors for improved power factor operation are presented. Typical experimental results obtained on a laboratory-size machine are also presented.

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Thesis Abstract (Ph.D.)

Spectral domain approach to electromagnetic modelling of wire and surface geometries by Syed Asadulla Bokhari.
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1. Introduction

The analysis of radiation from wire antennas in the presence of finite bodies has been generally carried out through the two well-known numerical methods, namely, the Method of Moments[1] and the Geometrical Theory of Diffraction[2] (GTD). The Method of Moments being primarily limited by available computational resources has been applied extensively for electrically small scatterers. On the other hand, the GTD which is based on the ray-theoretic approximation has been found to be well suited for electrically large scatterers. Owing to the limitations of these methods, the need for numerical techniques applicable in the "intermediate range" has been called for. One of the methods which has shown considerable promise in this direction is the Spectral Iteration Technique[3–4] (SIT). The method derives its computational advantages through a formulation of the integral equation in the Fourier transform domain, coupled with an efficient iterative scheme using the FFT algorithm.

The work reported in this thesis concerns a study of the SIT for the analysis of wire antenna geometries in the presence of finite bodies. Theoretical investigations that have been carried out encompass problems involving current distributions in one, two and three dimensions.

2. Analysis of wire antennas and arrays of wire antennas

The problem of analysing thin-wire antennas has been tackled using the SIT[5]. The SIT has been interpreted in terms of the method of moments. This interpretation has given more insight into the mechanism by which the SIT derives its computational merits as compared to the moment method solutions. Convergence criterion for the iterations has also been derived. From this it has been observed that the iterations converge well as long as the sampling interval is not too small. A numerical study of the convergence has also been carried out. An interesting result obtained is that the convergence of the iterations is ensured for wire lengths in the neighbourhood of the half wavelength. Several examples of wire antenna parameters have been illustrated to bring out the effectiveness of this method.

The interpretation of the SIT in terms of the method of moments has revealed that the expansion functions employed in the computation are of the piecewise-constant type. A method to extend the SIT to incorporate a more general class of expansion functions has been developed[6]. A unique feature of this technique is that a significant improvement in the convergence of the results obtained by the SIT can be achieved with a minimum of extra computations, while retaining all the advantages of the SIT. The input impedance of thin-wire antennas has been evaluated using the modified SIT wherein expansion functions of the piecewise-sinusoidal type have been made use of.

In order to tackle the problem of analysing arrays of wire antennas, a modified-stacked SIT has been evolved[7]. It has been found that the existing version of the stacked SIT is not directly well suited for treating wire antenna arrays owing to the wrap-around properties of the discrete Fourier transform. A modified procedure in which mutual coupling between the elements has been accounted for in the spatial domain has been developed. This technique together with the piecewise sinusoidal expansion for the current distribution has been found to be well suited for handling large arrays. Numerical examples have been worked out for the Yagi-Uda array to illustrate the technique.

3. Analysis of wire antennas on finite bodies

For handling monopoles mounted on flat surfaces, it is necessary to account for the continuity of the current at the wire-attachment point[8]. Therefore, a disc attachment mode, which leads to the problem of a monopole at the centre of a circular ground plane has been investigated[9]. The integral equation for the current distribution on the disc has been formulated in the Hankel transform domain and the solution has been obtained using the SIT. Available Hankel transform algorithms have not been found to be suitable for this application mainly because they do not ensure reciprocity in the transformation. An algorithm which circumvents this difficulty and is well suited for the present problem has been developed. Furthermore, closed form expressions for the fields of a magnetic frill source current have also been derived in the Hankel transform domain. It has been observed that for the accurate computation of the current distribution on the disc, a very fine sampling is required mainly due to the rapid variation of the disc current in the neighbourhood of the wire-attachment point. A technique similar to the singularity subtraction method has been developed to overcome this difficulty. Results of the current distribution and the far-field patterns have been presented.

The problem of radiation from monopoles on finite-size rectangular ground planes has also been tackled[10]. The usage of two-dimensional piecewise-sinusoidal expansion functions with the SIT has been illustrated for the problem of plane-wave scattering by a rectangular plate. The disc attachment mode has been employed to treat monopoles on finite-size ground planes. Extensive results of radiation patterns and current distributions as a function of the plate size have been presented. A discussion concerning the difficulties encountered in the accurate evaluation of the input impedance of wire antennas on finite ground planes has also been included.

A problem involving the current distribution in three dimensions has also been considered[11]. It has been observed that in such situations, the repeated application of the two-dimensional formulation does not possess a significant computational advantage. Therefore, an iterative solution in the three-dimensional Fourier transform space has been adopted for this purpose. Radiation patterns of a Hertzian dipole in the presence of a cube-shaped body have been evaluated and compared with the results obtained by the GTD.

Comparisons of the results obtained in this work have been made with those available in the literature -- either based on other numerical techniques, or measurement, and good agreements have been observed. The computational efficiency of the present formulation has been found to be substantial as compared with other known techniques.

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Thesis Abstract (M.Sc. Engng)

A token ring local area network for small systems application by V. Mustaq Ali.
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1. Introduction

This research work deals with a new design, and study of a token ring local area network (LAN) for small systems application like microcomputer network. The salient features of the work carried out are as follows:

- Development of a new access technique and a distributed algorithm to realize a token ring,
- hardware design and construction of a microprocessor-based ring interface unit and an experimental ring net,
- construction of a traffic-adaptive simulation model with a cyclic queuing procedure for performance evaluation and
- study of a multiple token ring which is modelled as separate single rings with a mixed class of stations.

Many access techniques have been developed to satisfy the requirements of a local area network[1], but the token ring has turned out to be the most suitable scheme for different applications ranging from office automation to real-time systems like process control. Numerous comparative analyses have proved the performance superiority of the token ring over the other schemes. The analysis has also shown the robustness of the token ring to the large variation in the network parameter and traffic[2]. However, as far as small systems applications are concerned, the realization of a token ring becomes quite complex in its control procedure, and relatively expensive mainly due to lack of an LSI implementation of this access scheme. In this work, a new and simple approach is described for designing and implementing an inexpensive token ring system. Also, modelling and performance studies of the ring net are done in a more realistic small-systems environment.

2. SDLC-loop-based token ring

Initially, in order to find a cost-effective approach to construct a ring node, standard data link protocols that are readily available in the form of low-cost single chip hardware are surveyed. As a result, the IBM-SDLC-loop protocol is found to be suitable due to the resemblance of its architecture with the token ring[3]. However, in the SDLC-loop architecture, the procedure of having a permanent primary station to control the entire loop generates an unbalanced traffic in the network; and poses reliability problems if the primary station fails. These are unsuitable features for a multi-user system like LAN. Therefore, to avoid these difficulties, in this work, all the SDLC stations are given an equal priority to control the loop. This is done by suitably modifying the SDLC-frame format and the polling procedure.

In accordance with these modifications, a distributed algorithm is developed to convert the centralized SDLC-loop architecture into a decentralized network like that of token ring. This algorithm allows the role of the primary station to circulate among all the stations in the loop. That

is, it permits any station to acquire this primary status when it has a message to transmit. After the loop transmit, the transmitting station is made to pass its primary status to the next access-seeking station, and thus making the loop control becomes distributed. To realize a loop station, an INTEL 8085 microprocessor-based Ring Interface Unit is constructed and it is tested in an experimental ring net. The network-control part of the system includes a protocol controller, a DMA controller, a transceive buffer, a clock recovery and a bypass circuit, and network command and control software.

3. Simulation modelling of token ring system

Although there exist numerous performance analyses on token ring, analyses pertaining to the study of the system in a realistic environment are scarce. In this work, a more general and versatile computer simulation model with a cyclic queueing procedure is constructed. In this model, it is observed that working with a single model (explicit or implicit polling type) to operate a wide range (0.1 to > 0.9) of network traffic is inefficient. For instance, in the case of a low-message arrival rate (<0.5), the execution time of the simulation program (of explicit polling) becomes prohibitively high. Because, a light traffic in the ring induces the circulation of idle-token for most of the time: a system state that does not contribute to the servicing of a message. Therefore, in order to improve the program's runtime efficiency, the model is broken into two different types—low and high-traffic models. Depending on the computational time of the previous run, the proper model is switched on for further simulation in the other ranges of traffic. This 'traffic-adaptive' simulation model reduces the overall CPU time of the program for all ranges of traffic[4]. Attempts are made to verify this simulation model by comparing it with known analytical results, and the results are found to be satisfactory. Apart from this varying traffic model, a saturated load (continuously queued) model is also developed. This aims to analyse the sensitivity of the token ring at extreme operational conditions.

4. Performance analysis of interconnected token ring

The simulation work is largely directed towards the modelling of the ring net in a more realistic small systems environment, *i.e.*, where the network is connected with a mixed class of stations like work-station, file-server, and bridge. This unbalanced traffic model is used to analyse multiple rings (2) which are connected by a bridge[5]. The flow of message between rings is characterized by an 'interaction-probability' with which a ring net transfers its messages to the other. This parameter is used to calculate the arrival rate of messages at a bridge-station of the ring net, and the multiple ring net is then modelled as logically separated single rings which have an unbalanced traffic in the net due to the presence of a bridge-station. While doing so, the delay history of the messages that arrive at the bridge-station from the other ring is properly accounted for.

The above analyses are mainly used to address the problems and to devise effective solutions to cope with the natural growth of stations in a ring net of a small systems environment. From different analyses, it appears that configuring a large single ring net into multiple rings connected by a bridge is a better choice than altering the existing capacity of the growing ring. Besides, in order to improve the throughput-delay efficiency of the multiple ring net, performance studies for various ring-interaction probabilities are done. The different techniques applied in this effort are: a) giving a 'priority-servicing' at the bridge-station, and b) applying a 'resource-balancing' approach in the ring nets to reduce the flow of many messages across the bridge.

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Thesis Abstract (M.Sc. Engng)

Errors and scaling in fast Fourier transform structures by V. Chander.
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Department: Electrical Engineering.

1. Introduction

Fourier transform is commonly employed in converting time-domain signals to their frequency spectra. Besides spectral analysis, it has been applied in many other areas[1] like astronomy, quantum mechanics, biomedicine and seismology. Discrete Fourier Transforms (DFT) can be considered to be a transformation of an N-data vector $x(0), x(1) \ldots x(N-1)$ into a new N-vector $X(0), X(1) \ldots X(N-1)$. With the advent of digital processing methods, general purpose computers have been employed for off-line Fourier transformation. Real-time processing, as in radar, sonar and communications, is realised by hardware. This requires reduction in number of arithmetic operations to achieve the required speeds. Fast Fourier Transform (FFT)[2] is an algorithm for implementing reduced number of multiplications in the DFT. The former requires only $(N/r) \log_r N$ multiplications versus N^2 of the latter. Here r, called the radix, is such that the FFT output $X(.)$ is obtained by successive intermediate stages numbering $\log r^N$.

The performance of a digital signal processor is limited by its finite word-length representation/operations. This is due to: (*i*) the errors introduced in representing real-world analog signals as digital numbers, (*ii*) the errors in representing the coefficients characterising the signal processing functions and (iii) the errors due to limiting the word-lengths of outputs of the arithmetic operations.

Analysis of errors allows computing parameters like the dynamic range and signal-to-noise ratio of any digital signal processor. Two methods of analysis exist[3]. The deterministic method models the errors as worst use and leads to overly pessimistic results. This analysis becomes intractable even with only a small number of error sources. The statistical method, on the other hand, models the errors as additive noise sources characterised by a mean and variance, and employs linear system theory for analysis.

This work analyses only the arithmetic errors in FFT as the errors due to input and coefficient quantisations are well understood[4]. Addition and multiplication are the two arithmetic operations

in all digital signal processors. FFT processors have, in addition, a third operation called scaling. Scalers prevent overflow in adders and are realised by a right shift or dividing by 2. Commonly used scaling methods[4] are: (i) prescaling all data $x(.)$ and (ii) Automatic Array Scaling (AAS) of each intermediate stage. A third method, called Conditional Array Scaling (CAS), scales intermediate stages only if any result at that stage is likely to overflow. This method is uncommon due to increase in control hardware.

This work (i) analyses the arithmetic errors in FFT processors employing radix-2 fixed-point arithmetic, and (ii) introduces a new scaling technique called Selective Conditional Array Scaling (SCAS) and brings out its alternative properties of lower error.

2. FFT error analysis

The basic operation in the Decimation in Time (DIT) and Decimation in Frequency (DIF) FFT flowgraphs is a butterfly. The inclusion of scalars results in new butterfly structures.

The scaling can be done before or after the butterfly giving the scaling-before-butterfly (SBB) and scaling-after-butterfly (SAB) structures. It is possible to interchange the order of cascading the twiddle factor multiplier and the scaler when they are on the same side of the butterfly *viz.* for DIT-SBB and DIF-SAB. Out of the four possible structures only three are realisable (DIT-SBB1, DIT-SBB2 and DIF-SAB as shown in fig. 1).

It is also possible to combine the multiplier and scaler operations into a single multiplier. This structure has been called Integral Scaling and Quantisation (DIT-ISQ).

Expressions for the errors at output of FFT flowgraphs for radix-2, employing all the above butterfly structures have been derived, in terms of the mean and variance of error sources due to multipliers and scalers. The results indicate that (i) the mean error at each output $X(k)$; (ii) the mean square error at each output; (iii) the total mean square error across all outputs.

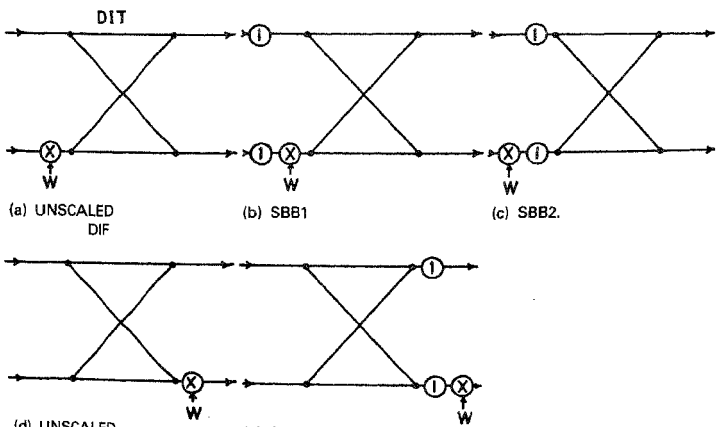

FIG 1. Butterfly structures.

The derivation employs the properties of flowgraphs and the Parseval's relation.

Previous work in the analysis of arithmetic errors was limited to sign magnitude and 1s complement arithmetics only. In all cases 'approximate' results were derived with no difference for DIT or DIF. Analytical results[5] for 2s complement arithmetic have been limited. Thong[5] considers only one type of butterfly structure (SSB) with no reference to practical realizability.

As the analytical expressions derived in this work are general in form and can be used for any type of arithmetic, *viz.* sign-magnitude, 1s and 2s complement. The derivations make only assumptions pertinent to practical butterfly structures and FFT flowgraphs *e.g.* trivial multiplications at end stages of the flowgraphs are accounted.

The analytical results were verified by simulation on a mainframe computer. The finite word-length hardware was implemented by programming the quantisation effects of the scaler and multiplier operations in the FFT butterfly. The program permits the choice of truncation or rounding as the quantisation method.

2.1 *Conclusions*

It is seen from the analysis and verified by simulation that

(i) the SAB structure has lower error than (nearly half of) SBB;
(ii) DIT-ISQ is superior by a further factor of 3;
(iii) Scaling contributes a larger share to the total output error. Hence conditional scaling methods are to be employed if possible.

3. Selective conditional array scaling (SCAS)

The study of scaling, which is the main contributor to the overall error, has led to the proposal of a new scaling method called Selective Conditional Array Scaling (SCAS). This method exploits the structure of the DIT and DIF flowgraphs.

AAS and CAS scale all the butterflies in a stage and can lead to the suppression of weaker signals in the presence of stronger ones. This is an important point in detection type of systems—detecting lines in the presence of broadband background. The SCAS scales at any stage selectively— only a block of butterflies. This confines the scaling errors to these blocks only.

The concentration (increased scaling) of scaling around the sharp lines leaves the other points of the FFT output unscaled or scaled less. In other words, more scaling error is introduced at higher amplitude sharp lines and less error at flat (non-sharp) regions. This property of SCAS is responsible for avoiding suppression of weak signals by the scaling errors when stronger lines are present. This spectrum adaptive nature is also demonstrated.

The SCAS procedure was simulated to study its effects. An interesting conclusion is—at the worst, SCAS is equivalent to CAS, and at the best to no scaling. The spectrum-adaptive nature of SCAS is also demonstrated.

The output of the FFT employing SCAS has a floating-point type of representation due to a different scaling at each element. The increased dynamic range, however, does not require a floating-point hardware in its implementation. A fixed-point hardware scheme requiring no more than N by log M bit memory (RAM) additionally (to an AAS-FFT) and some control hardware is also explained.

3.1 *Conclusions*

(i) SCAS is a spectrum adaptive scaling method;

(ii) It is superior to CAS;
(iii) Realisation of SCAS is practicable.

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Thesis Abstract (M.Sc. Engng)

Automatic generation of power system one-line diagrams by N. Raman. Research supervisors: K. Parthasarathy, H. P. Khincha, P. G. Kharche. Department: Electrical Engineering.

1. Introduction

Modern power systems have grown in size and complexity. Manual methods of analysis, design and presentation of results are becoming obsolete with the widespread use of computer graphics in the area of power systems. Computer graphics is used to provide a visual picture of the system configuration and state by means of power system one-line diagrams. With the advent of computer-based digital control systems, schematics displayed on CRTs serve as the new operator's window to the process[1]. One of the recent trends in this area is that the wall diagram (mimic) is being replaced by a computerised version which improves control capabilities over the system[2]. Power system one-line diagrams are extensively used in the areas of planning and operational studies.

2. Methodology adopted

Power system one-line diagrams serve as an effective and convenient means of representation of power system networks. The objective of the present work is to develop a methodology for automatic generation of one-line diagrams. By 'automatic generation', it is implied that the various steps involved in the layout of the one-line diagram can be computerised, once certain basic inputs have been provided. Since it is desirable to have the network geographically oriented, the geographical coordinates of buses and the network connectivity are considered as basic inputs. The various steps involved in the automatic generation process are identified as: bus positioning, bus orientation, arrangement of interconnections, minimisation of crossings, length of the bus drawn, insertion of results of load flow and general plot control parameters.

2.1 *Bus positioning*

A bus-positioning algorithm has been developed to meet the following objectives:

a) To retain the relative geographical locations of buses to the extent possible;

b) To generate a uniformly spaced layout;
c) To compute the coordinates of buses as drawn.

2.2 *Bus orientation*

In a conventional power-system one-line diagram, the buses are drawn either horizontally or vertically[3]. This choice can be made automatically by the program based on the connectivity pattern of the network and the bus positions.

2.3 *Arrangement of interconnections*

An algorithm for optimal arrangement of interconnections has been developed. Both branch and shunt connections are considered. The branches are sorted based on the angles of interconnecting branches and are separated into two categories *viz.*, top or bottom for horizontal buses and left or right for vertical buses.

2.4 *Minimisation of crossings*

One convenient quality index regarding the aesthetics of a schematic is the number of line intersections or crossings[4]. Here, two types of crossings are of interset. The first type is the crossings between a bus and a branch; the second type is the crossings between branches. The objective here is to completely eliminate the crossings of the first type while minimising the crossings of the second type. The techniques used for achieving this include adjusting the take-off distance, shifting or interchanging the take-off positions of branches on the bus, adjusting the distance between adjacent connections or by permutation of bus positions.

2.5 *Length of the bus drawn*

The length of the bus drawn is calculated based on the maximum number of branch connections on either side of the bus. The shunt connections are added so as to even out the number of connections on both sides of the bus. This approach ensures that the bus length is kept to the bare minimum required by the connectivity of the network.

2.6 *Insertion of results of load flow*

One of the main aims of automatic generation of one-line diagrams is that the results of system studies can be displayed directly on the diagram. This is demonstrated in the present work, by considering load flow study as an example. The one-line diagram generation program has been interfaced with a standard load-flow program. The load flow results are plotted on the diagram.

2.7 *Plot control*

Several plot control features have been provided which can be effectively used to control the overall appearance of the diagram. Some of the input parameters are:

i. Distance between adjacent branches on the bus
ii. Distance between the last branch and the end point of the bus
iii. Minimum take-off distance
iv. Sizes of symbols and text
v. Scale factor for scaling the entire diagram
vi. Standard paper size: A1, A2, A3, or A4
vii. Option for plotting the diagram with or without grids
viii. Option for plotting the diagram with or without results

3. Conclusions

The algorithms developed have been implemented in a detailed prototype computer program, written in Fortran-77. The software provides a plot of the one-line diagram with load-flow results. Specific advantages of this approach are that the resulting diagram is geographically oriented and that the results are obtained with least manual intervention. Areas in which such a procedure will be applicable are:

a) As a stand-alone program for engineering use.
b) As a front-end processor of an interactive analysis package.
c) As a display aid in the operation of an energy control centre.

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Thesis Abstract (Ph.D.)

DPSK MODEMS and synchronisers: Some new realisations by H. S. Jamadagni.
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1. Introduction

Data MODEMs are building blocks required in data networks for transmission of data on analogue transmission media. As data transmission is now playing a vital role in computer communication systems, data MODEMs are assuming great importance. MODEMs with bit rates greater than 9.6 kbps are usually realised as base-band MODEMs. On the other hand, MODEMs with lower bit rates (*i.e.*, 9.6 kbps and less) use some form of modulation as they are mainly used for data transmission over the telephone network. The early MODEMs were based on Amplitude Shift Keying (ASK) and Frequency Shift Keying (FSK). However, their performance had many limitations in the presence of noise and line imperfections. Hence, their use has been limited to low data rates (1200 bps and less). The use of Phase and Differential Phase Shift Keying (PSK and DPSK) lead to high performance MODEMS compared to those based on ASK and FSK. However, they call for a complex hardware, which was difficult to realise in the early days.

With the advent of digital ICs, it is now possible to realise complex hardware at a low cost. Hence, the development of All-Digital MODEMs assumes importance. Furthermore, the DPSK scheme merits a detailed study, because of its growing importance in MODEM design. Hence, an in-depth study on realisation of all-digital DPSK MODEMs along with the synchronisers needed was taken up.

2. Results and discussion

This study has led to the realisation of two new forms of all-digital DPSK MODEM and three novel types of synchronisers, with a performance almost the same as that of the theoretical scheme using analogue circuits. Not only theoretical analysis but also computer simulation and experimental work have been carried out in this study. The demodulators developed here (referred to as the Integrate-And-Dump (IAD) and Limiting integrator-type demodulators) are highly suitable for LSI/VLSI realisation. Important results of this study are summarized below:

2.1 *DPSK demodulator*

2.1.1 *Analytical study*

A new method of analysis of all-digital DPSK demodulator has been developed. The main results of this analysis are:

- The IAD scheme is amenable to simple analysis, which leads to a good understanding of the demodulation process;
- The above analysis can be easily extended to the limiting integrator demodulator.

2.1.2 *Computer simulation*

A novel modular programme has been developed to evaluate the BER values of different types of DPSK demodulators. The main results of this simulation are as follows:

- The BER performance of IAD demodulator, the limiting integrator type of demodulator and Lawrence's demodulator are nearly the same as that of the theroretical analogue scheme over a wide range of values of SNR;
- Even a general non-linearity of the type which can replace the hard limiter (Schimtt trigger) at the input of the proposed demodulators, has no significant effect on their BER performance;
- The use of an adaptive circuit (to predict the expected noise) does not offer any significant advantage over the simpler IAD and limiting integrator demodulator schemes.

2.1.3 *Experimental studies*

Analytical studies and computer simulation have been used to develop all-digital DPSK demodulators, which are realised using standard LS TTL ICs. The main results of this work are given below:

- The demodulator using the limiting integrator behaves as a matched filter for the DPSK signal;
- The BER of the demodulator is critically dependent on the limits chosen;
- The IAD demodulator needs a separate synchronisation circuit for its operation which is more complex than the demodulator itself;
- The BER performance of the demodulator developed is comparable to that of the theoretical analogue demodulator;
- A VLSI based on the circuit developed here is feasible. A silicon area of the order of 4 sqmm is required for realising this.

2.2 *Synchronisers for DPSK schemes*

Different synchroniser topologies were developed for the DPSK demodulator. Of these, it is observed that the near-ideal Maximum-APosteriori (MAP) and Data Transition Tracking Loop

(DTTL) synchronisers have a superior performance as compared to the simpler Early-Late-Gate synchroniser.

2.2.1 *Analytical study*

Synchronisation in a receiver, in essence, uses parameter-estimation techniques. The following points emerge from the derivation of synchronisers using the estimation theory:

– The MAP estimator, which is frequently used in many applications, is also suitable for the DPSK scheme;

– The ideal MAP synchroniser is too unwieldy to realise in practice. However, simplifications can be introduced to yield simple synchronisers, which are easily realised;

– DTTL is an alternative form of the MAP synchroniser, which is also easy to realise;

– The Early-Late-Gate synchroniser is a gross approximation to the DTTL scheme.

2.2.2 *Computer simulation*

This simulation has yielded the following important results:

– The near-ideal MAP synchroniser is indeed an excellent synchroniser for the DPSK scheme. The use of this synchroniser does not degrade the BER performance of the demodulator above 4dB of SNR;

– The acquisition property of this synchroniser depends on the LPF bandwidth used. Hence, with a proper choice of this parameter, the acquisition is within about 12-bit periods;

– The DTTL is also a very good synchroniser for the DPSK scheme. However, it is more complex to realise than the MAP scheme. It also takes more time for synchronisation and shows a remarkable oscillatory tendency;

– The Early-Late-Gate synchroniser performance is inferior to that of the MAP and DTTL synchronisers. In fact, the degradation in BER is about 1.5dB of SNR;

– The jitter produced by all the synchronisers is almost Gaussian distributed, particularly at low SNR values.

2.2.3 *Experimental study*

Realisation of the MAP and DTTL synchronisers is relatively complex. Hence, the use of a microprocessor is almost mandatory for their realisation. The results of experimental studies on microprocessor-based synchronisers developed are given below:

– The MAP synchroniser is easier to realise than the DTTL synchroniser;

– The matched filter required in the MAP synchroniser can be realised with the help of a limiting integrator demodulator;

– The integrators needed in the DTTL synchroniser can be realised using two IAD demodulators;

– The LPF bandwidth and loop gains have to be chosen carefully for the operation of these synchronisers;

– Incorporating the synchroniser in a VLSI for DPSK MODEM calls for designing a special-purpose microprocessor, which appears to be technologically feasible in the same chip as the MODEM circuitry. The estimated silicon area for this is 10 sq mm.

Reference

1. JAMADAGNI, H.S. *et al* A new method of calculation of BER of DPSK systems. Les Arcs: *IEEE Conf. Inf. Theory*, June 1982.