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SOI sensors and epitaxial MEMS[†]

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Abstract

This paper reviews the development of pressure and acceleration sensors using SOL wafers. SOL structures help in high-temperature operation and simplify the fabrication process. MEMS technology and devices studied in the author's lab are also presented.

Keywords: SOI, sensor, epitaxial, MEMS, Si.

1. Introduction

Si-on-insulator (SOI) structure is an attractive material both for VLSI and sensor applications. SOI structures for VLSI substrates are usually fabricated with single crystal Si(100) layers/SiO_2 layers on Si(100) substrates such as SIMOX wafers (separated by implanted oxygen) and SDB (silicon direct bonding) wafers. For sensor applications, SDB wafers have many advantages over SIMOX wafers as the thickness of the top Si layer can be changed to a few hundreds of μm from 0.1 μm. A μm-thick SiO_2 layer is also available. Top Si layers can be used as piezoresistor or proof-mass and SiO_2 can be used as an electric isolation or a sacrificial layer. On the other hand, epitaxially stacked SOI structures, such as Si/Al_2O_3/Si structures, which can be formed by using epitaxial Al_2O_3 on Si substrates and epitaxial Si on Al_2O_3/Si, can be used as sensor material. Using epitaxial method, the thickness of Si and insulator layers can be controlled easily for sensor applications. MultiSOI structures like Si/insulator/Si/insulator/Si structure can be formed and are of interest for micromachining.

In this paper, using the above-mentioned SOI wafers, a pressure sensor and an acceleration sensor have been developed. Some of the advantages of SOI are high-temperature operation of sensors up to 300°C and simplification or controllability of fabrication process.[1] We also present MEMS technology and devices studied in our laboratory.

2. High-temperature-operated SOI pressure sensors

2.1. SOI pressure sensors

High-performance pressure sensors which can be used at temperatures as high as 300°C and in corrosive environments are in demand in many fields such as automobile engine control, subterranean heat exploration and industrial pressure instruments. The most promising structures for such high-temperature-operated sensors are SOI structures where strain gauges are isolated electrically from Si substrates by dielectric layers. Therefore, even at temperatures above 120°C, the

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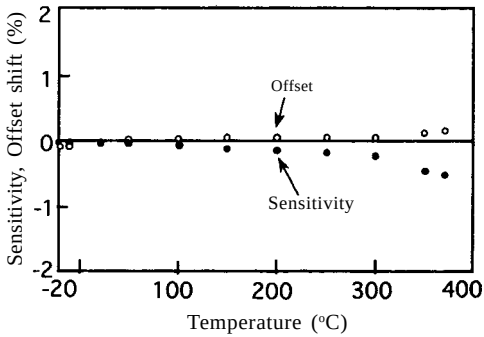


FIG. 1. Temperature characteristics of sensitivity and offset voltage of SOI pressure sensors.

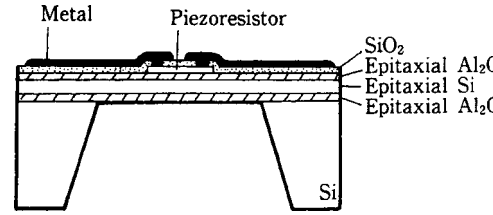


FIG. 2. A double SOI structure pressure sensor with Al_2O_3.

electrical isolation is perfect and the device can operate up to 300°C (Fig. 1). The usual Si device isolated by pn-junction does not work above 120°C due to increased leakage at the pn-junction.

The insulator layer can also be used as an etching stop layer to make a diaphragm. This is another advantage of the SOI pressure sensor. Several kinds of sensor structures were reported using $Si/Al_2O_3/Si$ structures by low-pressure chemical vapor deposition (LPCVD) method.[2] Figure 1 shows the temperature characteristics of sensitivity and offset voltage of SOI pressure sensors. The values of sensitivity and offset voltage are less than −0.2% and +0.1%, respectively.

2.2. *Double SOI pressure sensors with Al_2O_3 and Si*

A piezoresistive pressure sensor for high-temperature operation was demonstrated with a double SOI structure consisting of four epitaxial layers of Si and Al_2O_3 films: a (100) $Si//Al_2O_3(100)//Si(100)//Al_2O_3(100)//Si(100)$-substrate stacked structure (Fig. 2.)[3,4] Its advantages are as follows: (1) Piezoresistors can be isolated electrically by the third-layer Al_2O_3 instead of pn-junction. (2) Accurate and uniform control of thin diaphragm could be achieved using the first Al_2O_3 layer as an etching stop layer as Al_2O_3 is more stable compared to Si anisotropic etching of KOH solution.[5] The second epitaxial Si acts as a thickness and strain-adjusting layer of the diaphragm. (3) Thickness of these layers is easily controllable due to epitaxial growth by CVD. (4) As the Al_2O_3 is stable and mechanically strong like sapphire, the SOI structure is compatible with the IC process.

FIG. 3. Photograph of a sensor.

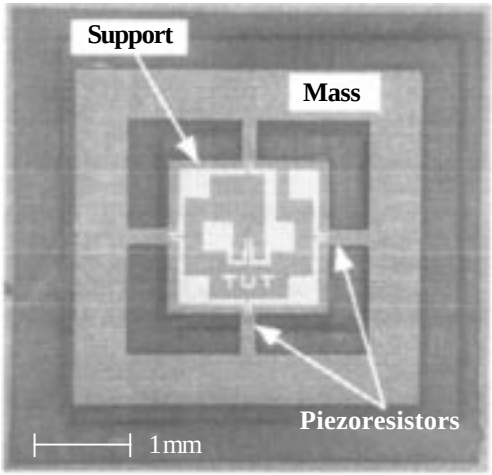


FIG. 4. Chip photograph of fabricated SOI accelerometer for high-temperature operation.

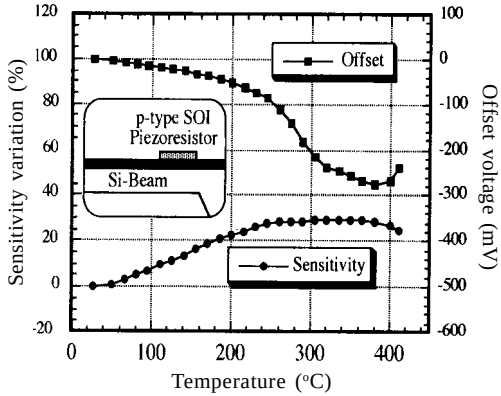


FIG. 5. Temperature characteristics of the fabricated SOI accelerometer.

2.3. *Device fabrication*

Figure 3 shows a sensor body. The sensor chip is mounted on the glass base (Hoya, SD-2) by anodic bonding and hermetic sealing.[6] Au wire is used to bond between the electrodes on the chip and pins of the hermetic seal. The stainless diaphragm is then welded. The cavity between the sensor chip and the stainless diaphragm is filled with silicon oil (Toray, SH710). Pressure is transmitted to the sensor chip through the silicon oil.

Since the primary resonance frequency is about 9 kHz, the sensor chip can be placed quite close to the stainless diaphragm. A study of long-term stability of the sensor was made. Offset and sensitivity of the sensor were measured at 200°C every five hours for 45 hours. The output change is less than 0.1% FS, both offset and sensitivity. This sensor may be stable up to 260°C in the short term. The silicon oil gradually gels more than 260°C (Table I).

3. Three-axis accelerometer

3.1. *Piezoresistive three-axis accelerometer using SDB-SOI structure for high temperatures*

Usually, the maximum operation temperature of piezoresistive silicon sensors is limited to 125°C due to higher leakage of current from junction-isolated piezoresistors. We have developed SOI mechanical sensors such as pressure sensors and accelerometers for high-temperature operation.[7]

Table I
Characteristics of a sensor

Characteristics	Measured values
Sensitivity for X, Y input	16 μV/V.G
Sensitivity for Z input	91 μV/V.G
Maximum cross-axis sensitivity	5.7%
Maximum nonlinearity	1.7% FS

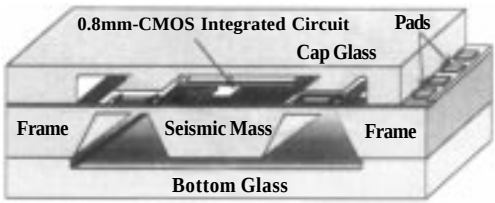


FIG. 6. Cut-away simplified drawing of the 0.8 μm-CMOS integrated three-axis accelerometer.

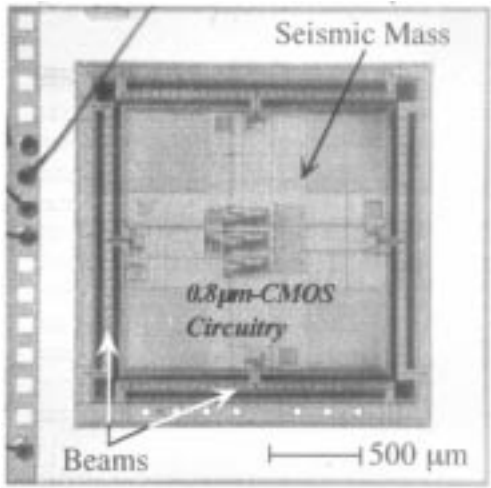


FIG. 7. Chip photograph of fabricated three-axis accelerometer ($3 \times 3 mm^2$).

Figure 4 shows the photograph of the chip of an SOI accelerometer developed for high temperatures. In the accelerometer, piezoresistors are isolated by silicon dioxide layer. Thus, leakage of current at high temperatures is eliminated perfectly. Furthermore, the accelerometer is designed to detect three-axis acceleration by operating the output voltage of four SOI piezoresistors. Temperature characteristics of the accelerometer were measured in the range from room temperature to 400°C. Figure 5 shows temperature characteristics of offset voltage and sensitivity variation. The data were standardized at 27°C. While the characteristics of typical junction isolated accelerometer change rapidly over 200°C due to dramatic increase in the junction leakage current, the SOI accelerometer was relatively stable up to 400°C. This shows the potential of SOI sensors to evaluate the basic charateristics of high-temperature SOI accelerometers.

3.2. *A three-axis accelerometer integrated with commercial 0.8 μm-CMOS circuits*

Our group has established the postCMOS fabrication technology for CMOS integrated three- axis accelerometer.[8,9] The integrated circuitry in the device was fabricated with commercial 0.8 μm-CMOS technology.[10] Because of its versatility, the technology can be applied for advanced deep submicro CMOS technologies. Details of the technology of fabrication principles and characteristics of fabricated devices, and reliability of the sensor devices have been reported in IEEE MEMS2000.[10]

Figure 6 shows cut-away simplified drawing of the 0.8 μm-CMOS integrated three-axis accelerometer. The device has a three-layer structure with a silicon layer sandwiched by two SW-3 glass layers. The cap glass is bonded on the surface of silicon structure to seal the accelerometer. Plastic can be used for low-cost packaging of the accelerometer. On the silicon surface, CMOS integrated signal processing circuits are integrated with commercial 0.8 μm-CMOS technology on the surface of the seismic mass. For detection of acceleration, p-MOSFETs are used as stress-sensitive elements. It is based on piezoresistive effect of p-type inversion layer in p-MOSFETs. Since p-MOSFETs are standard elements in standard CMOS circuits, they can be used as sensing

elements in CMOS integrated sensors. Figure 7 shows the photograph of a fabricated three-axis accelerometer with $3 \times 3\ mm^2$ dia area. At this stage, cap glass is not bonded on CMOS surface. The minimum measured resolution of the accelerometer with $6 \times 6\ mm^2$ chip size is about $2.0\ mG_{rms}$ for Z-axis acceleration, and about $26.8\ mG_{rms}$ for $3 \times 3\ mm^2$ accelerometer. Basic performance characteristics including reliability of repetitive application of load were quite good, probably because of smaller scaled integrated circuits.

4. Capacitive SOI accelerometers

4.1. *Surface micromachining method*

Capacitive accelerometers using SDB-SOI (silicon direct bonding–silicon on insulator) structure have been developed recently.[11–16] The silicon thickness of SDB–SOI wafer is controlled by polishing which gives desirable thickness from hundreds of microns to a submicron. By using trench (deep) etching technology, thick (over 10 μm) and high aspect structure can be formed with SOI wafer. Intermediate SiO_2 layer acts as etch-stop layer for deep etching process, which can also be used as sacrificial etching layer. The thick and high aspect structure gives higher sensor capacitance and heavier mass compared to the conventional polysilicon surface micromachining accelerometer. The beams with single crystal silicon raise reliability as they do not have hysteresis or creep, and hence the SOI structure is considered attractive for MEMS sensors.

One-axis capacitive accelerometer and three-axis accelerometer have been developed using SOI technology.[17] Figure 8 shows the three-axis SOI capacitive accelerometer. Z-axis accelerometer is of 1×1 mm size and the spiral shape beams are 2–3 mm in length. The thickness of the top

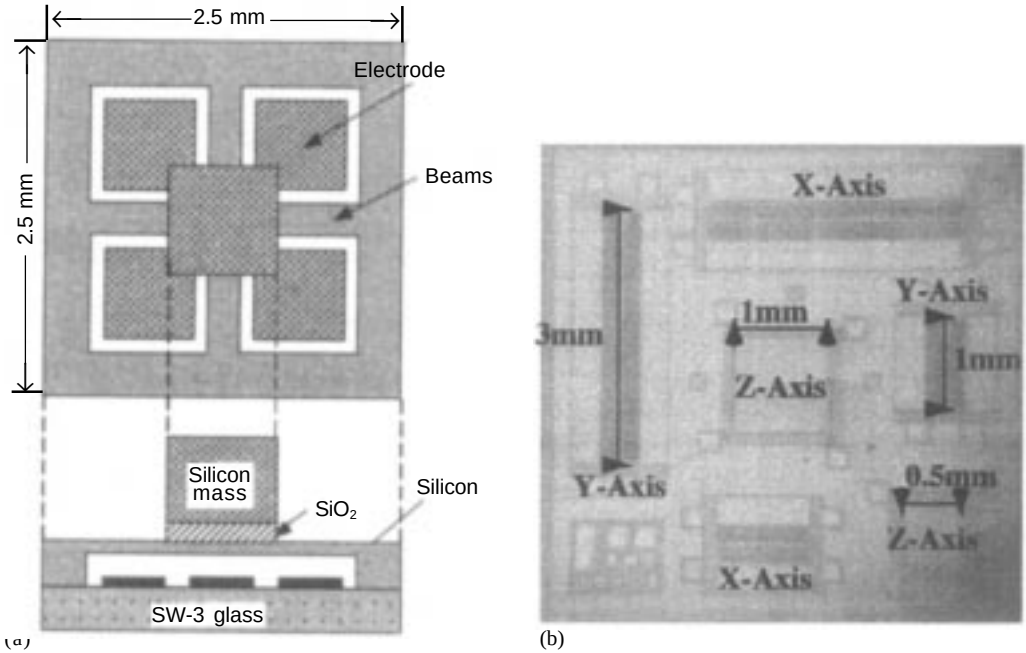


FIG. 8. (a) Structure and (b) SEM images of SOI three-axis accelerometer.

single-crystal silicon layer is 6 μm and the gap, i.e. the sacrificial silicon dioxide layer is 1 μm thick. X- and Y-axis accelerometer is of 3x1 mm size and folded beams are 1–2 mm in length. The length of the comb electrode is 200 μm and a gap of 4 μm is maintained between the electrodes. Initial sensor capacitance is about 5pF for Z-axis accelerometer and 2pF for X- and Y-axis accelerometer. The total design size of the sensor is 5x5 mm.

4.2. *Dicing saw method*

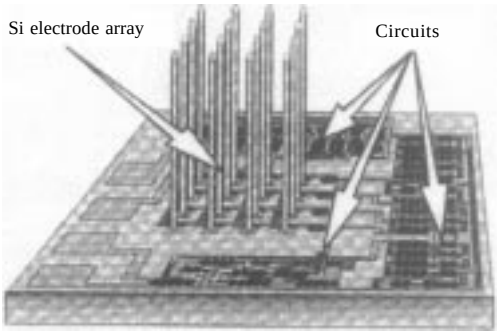
Novel three-axis SOI capacitive accelerometer has been designed for low-G detection. It has a mass of over 500 μm thick formed by dicing saw using bulk silicon substrate. The mass can be formed in high aspect ratio of nearly infinity using a dicing blade of a width of 500 μm. It promises high sensitivity for each axis acceleration and small sensor size of 2.5x2.5 mm. The capacitor electrodes were designed in clover-leaf structure using SOI structure. The electrode forms a differential capacitor for X- and Y-axis accelerometers, which is effective to reduce noise or temperature dependence.[18,19]

The structure of the three-axis accelerometer is shown in Fig. 8. It has a mass of over 500 μm thickness formed by dicing saw on the glass–silicon structure. The mass is supported by thin (less than 10 μm) single-crystal silicon straight beams or spiral silicon beams. The mass forms a common electrode. A Z-axis accelerometer is formed between the mass and the metal electrode on glass substrate. Clover-leaf silicon plates are attached to the mass to form X- and Y-axis capacitors. X and Y accelerometers are formed between the clover-leaf plates and the metal electrodes on the glass. The base capacitance is about 1.5 pF and the capacitance changes from 10 fF/G to 100 fF/G. A high-performance capacitance detection ASIC including a switched capacitor circuit and a second-order delta-sigma modulator has been developed for the accelerometer.[20]

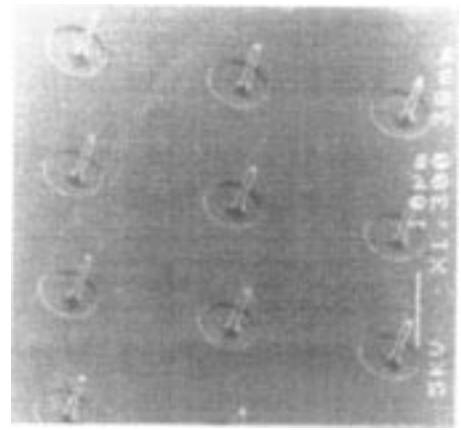
5. MEMS devices

5.1. *Intelligent potential sensor array with VLS growth method*

Ultrasmall Si wire array fabricated by VLS (vapor–liquid–solid) growth with nMOS circuits on the same chips was proposed using Si(111) wafers for application as a new intelligent nerve potential



(a)



(b)

FIG. 9. (a) Image structure of intelligent potential sensor and (b) SEM photograph of Si wire array.

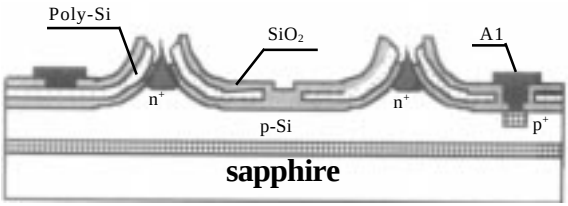


FIG. 10. Schematic cross-sectional view of the proposed photosensitive floating field emitter.

sensor. Selective epitaxial Si wires (8 μm high and 1 μm dia) with (111) orientation were successfully grown at 700°C for 2 h by Si_2H_6 gas source MBE using Au lift-off process (Fig. 9). The growth rate (1–11 μm/H) and diameter (1–4 μm) of the wire depend on Si_2H_6 gas pressure and Au pattern size (4–10 μm) and thickness, respectively. The characteristics of nMOSFETs on Si(111) are controlled by ion implantation and do not show any change except for increase in subthreshold current to 10^{-9}A at the MOSFETs with wires after VLS growth of 700°C. MOS circuits can be operated by this new process and the VLS growth and MOS IC process are compatible.[21]

5. 2. *Photosensitive floating field emitter*

A new photocathode termed 'photosensitive floating field emitter' was investigated.[22, 23] Back-incident-type photosensitive field emitter was fabricated using an SOS (silicon on sapphire) substrate. Schematic cross-sectional view of the proposed photosensitive floating field emitter is shown in Fig. 10. It is constructed with cone-shaped gated Si field emitter tips and pn-junction photodiode devices. This device structure can introduce lights efficiently from backside, as the sapphire substrate is transparent to ultraviolet, visible and infrared lights. A prototype, which was fabricated by depositing amorphous silicon pin photodiode films on the back of n-type cone-shaped Si emitter array, was fabricated and characterized. The emission current increases linearly as a function of the illumination intensity and the quantum efficiency was over 70%. This value is three times higher than that of conventional photocathode.

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