Output phase assignment for area and power minimization in PLAs

SAURABH CHAUDHURY* AND SANTANU CHATTOPADHYAY
Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology Kharagpur, Kharagpur 721 302, India.
email: (saurabh, santanu)@ece.iitkgp.ernet.in.

Abstract

A fairly good amount of optimization can be achieved in PLA-based two-level realization of circuits using a proper choice of phases for the subfunctions. This paper presents a genetic algorithm-based approach for selection of output phases to optimize the PLA for area and power. The results obtained are superior to those reported in the literature. Finally, a trade-off has been made to perform a weighted minimization of area and power. It has been shown that a range of solutions can be achieved with varying degree of area and power optimization using different weightages to the area requirement and the power consumption of the resulting PLA.

Keywords: Optimization, PLA, power minimization, genetic algorithm.

*Author for correspondence.