J. Indian Inst. Sci., May–June 2006, **86**, 215–233

Development of simple fuzzy logic controller (SFLC) for ZVS quasi-resonant converter: Design, simulation and experimentation

S. ARULSELVI[1]*, UMA GOVINDARAJAN[2] AND V. SAMINATH[3]
Department of Electrical Engineering, Anna University, Chennai 600 025, India.
email: [1]arulselvi_2k3@yahoo.co.in; [2]uma@annauniv.edu; [3]saminathmail@yahoo.com

Received on July 21, 2005; Revised on November 11, 2005.

Abstract

This paper presents the design of simple but powerful fuzzy logic controller (SFLC) based on single input variable instead of the process state variables or error and its derivatives to represent *n*-dimensional rule table as in the case of conventional FLC (CFLC). SFLC has only one-dimensional rule table, which in turn reduces memory requirement and computational complexity in coding. Also the tuning of scaling factors and the generation of fuzzy rules becomes easier. As a result, realizing fuzzy algorithm in a microcontroller or digital signal processor becomes simple. The application of SFLC is verified for voltage control of ZVS-QRC against load variations. The analysis, design and control characteristics of buck-boost ZVS-QRC are presented. The control performance of SFLC is compared with CFLC through simulation and experimental studies using 40 MHz, 16bit, TMS320F2407A DSP Processor. Results show improved performance of SFLC.

Keywords: Frequency-modulated zero voltage switching quasi resonant converter (FM-ZVS-QRC), proportional integral derivative (PID), sliding mode control (SMC), simple fuzzy logic controller (SFLC).

1. Introduction

PWM-based switched mode power supplies are used in telecommunication and aerospace applications. At high frequencies, these converters experience high switching losses, reduced reliability, electromagnetic interference and acoustic noise. To overcome these drawbacks, quasi-resonant converters (QRCs) are used [1–2]. QRCs utilize the principle of either zero current switching (ZCS) or zero voltage switching (ZVS). Due to reduced switching losses it is possible to operate the QRC at high frequencies, which in turn increase the power packing density and efficiency of the converter. The output voltage regulation of the converter against load and supply voltage fluctuations is an important criterion for designing high-density power supplies. To improve the speed of response and to achieve regulation, it is necessary to have a closed loop control system. The proportional integral derivative (PID) controller design for the voltage control of dc-dc converter based on average modeling has been reported [3, 4]. These controllers are sensitive to operating points and parameter variations. The complex structure and nonlinear control characteristics of

*Author for correspondence. Present address: Department of Instrumentation, Annamalai University, Chidambaram 608 002, India; Ph: 04144-237193; Cell: 9444191358.

QRC necessitate the design of nonlinear controller. Attempts have been made to achieve voltage regulation using sliding mode control (SMC) technique. The design of SMC does not require accurate mathematical model and it provides robustness against load and supply disturbances, whereas it produces drastic change in control variable which leads to chattering [5, 6].

Recently, the application of conventional FLCs (CFLCs) to control power electronic converters has been reported [7–10]. It does not require a precise mathematical modeling of the system or complex computations. This control technique relies on the human capability to understand the system's behavior and is based on qualitative control rules. It has the ability to extend the control capability even to those operating conditions where linear control techniques fail, i.e. large signal dynamics and large parameter variations. As the CFLC approach is general, the same control rules can be applied to several dc-dc converters with minor modifications in the scaling factor depending upon the converter topology and parameters. Hence, CFLC is a preferred tool for the control of complex structured nonlinear systems such as quasi-resonant converters compared to other control techniques.

In most of the converter applications, the design of CFLC is carried out based on a two-dimensional rule table to generate control signal. This technique has been reported through simulation studies for hard-switched converters and QRCs [11–14]. Some researchers have reported the experimental studies using either microcontroller or DSP processor [15–17]. The feasibility of CFLC design for hard-switched converter is discussed and implemented using a fixed-point DSP TMS320C50 [16]. It requires an external PWM generator, analog-to-digital-converter (ADC) and digital-to-analog converter (DAC) modules. The size of control rule table established is 5×5 with 25 rules, which requires an execution time of one millisecond. The application of CFLC for the control of hard-switched converters using an 8-bit microcontroller with 'ON-chip' ADC and PWM generator is reported [17]. The size of the rule table generated for this application is 7×7 with 49 rules. In this method the execution time is reduced to 250 microseconds but the maximum switching frequency is restricted to 31.373 kHz. The drawbacks of programming the microcontroller are unsigned integer arithmetic and limited memory space. Hence, an approximate method of defuzzification is implemented, which does not give comparable results if the centriod of output membership functions are far apart. It is observed from the above findings that the CFLC imposes the following constraints during hardware implementation: computational complexity in coding, increased memory space in proportion to the size of the rule table, difficulty in tuning of scaling factors and rules.

To overcome the above shortcomings, a simple FLC (SFLC) simulation procedure applicable for an inverted pendulum and magnetic levitation is proposed [18]. Real-time implementation of this technique has been reported for the voltage control of dc-dc boost converter [19–21]. This method has one-dimensional rule table derived based on skew symmetric property of CFLC rule table. A new fuzzy variable called *signed distance* is defined as input to the SFLC. It decides the magnitude of control signal for a given error (e) and change of error (ce). In the present work, SFLC control has been proposed for the voltage control of half-wave buck-boost ZVS-QRC using TMS320F2407A processor. It reduces the execution time, complexity in realizing the control algorithm during hardware implementation and memory space required compared to CFLC.

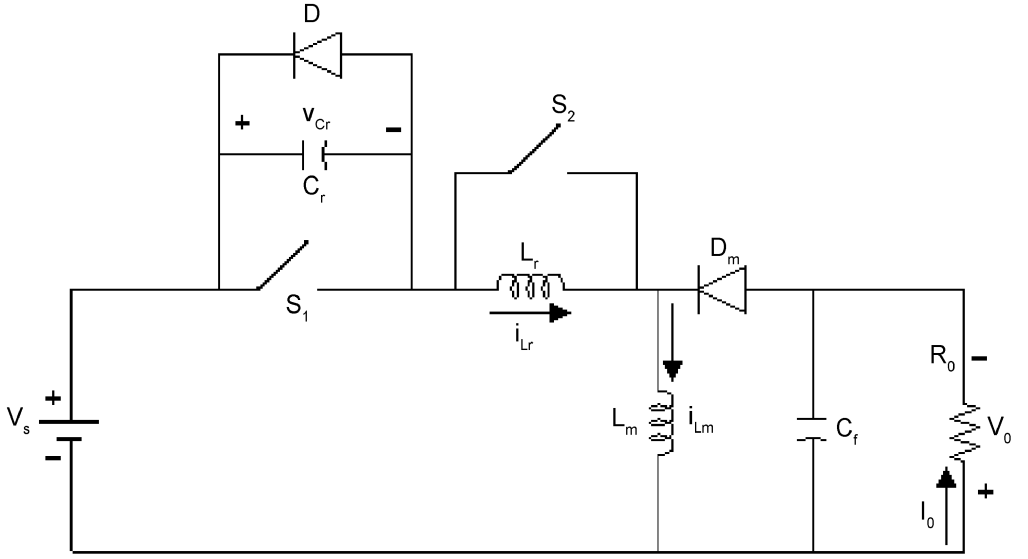

FIG. 1. Circuit diagram of buck-boost ZVS-QRC.

This paper is organized as follows: In Section 2, the detailed analysis, design and control characteristics of buck-boost ZVS-QRC are presented. The design of CFLC and SFLC is discussed in Section 3. Closed loop simulation results are presented and discussed in section 4. Section 5 presents the experimental results based on CFLC and SFLC. Section 6 concludes the work.

2. Analysis and design of half-wave buck-boost ZVS-QRC

The circuit diagram of buck-boost ZVS-QRC is shown in Fig. 1. The main switch S_1 and an auxiliary switch S_2 are connected in parallel with C_r and L_r, respectively. The conduction time of the main switch S_1 decides the buck or boost operation of the converter. The resonant inductor L_r and resonant capacitor C_r form the resonant tank circuit and they are used to shape the voltage waveform across the main switch S_1 in quasi-sinusoidal form. The effect of C_{ds} of S_1 and S_2 is not considered for resonance of buck-boost ZVS-QRC. D_m is a freewheeling diode, L_m, a magnetizing inductor and C_f, a filter capacitor. The filter capacitor is used to minimize the ripples in the output voltage. Both the switches operate under zero voltage condition.

2.1. *Analysis of ZVS-QRC*

The converter works in six different modes of operation in a switching cycle. The theoretical resonant waveforms of the converter for different modes under the steady state condition are shown in Fig. 2. It is seen that the switching cycle in ZVS topology starts with the main switch S_1 in the non-conduction state. Six modes of operation are explained [22, 23] by referring to Figs 1 and 2.

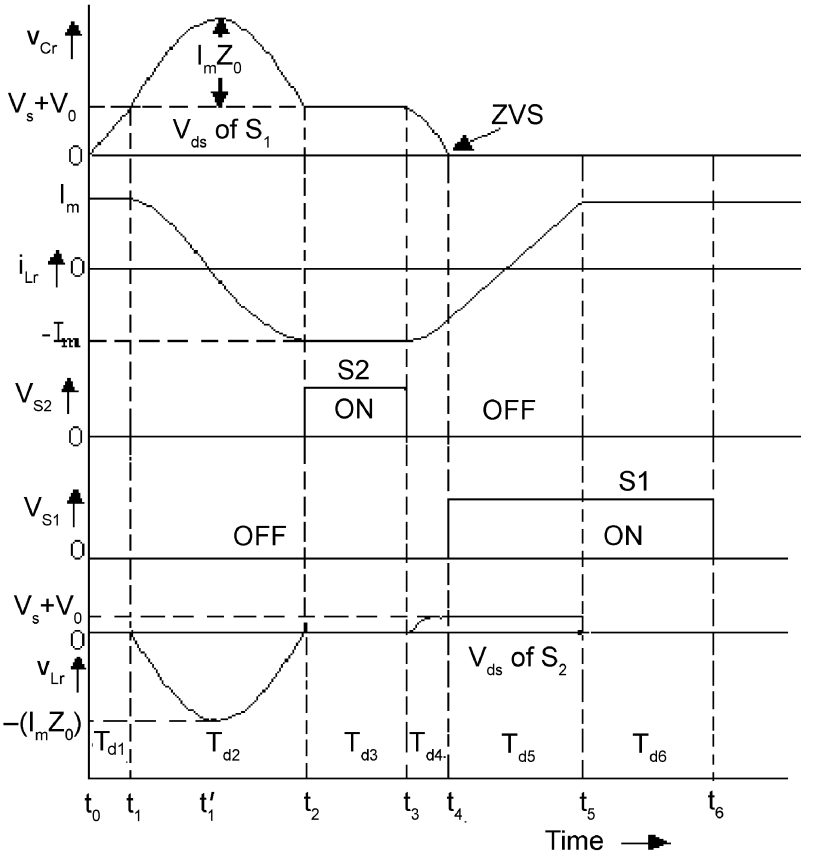

FIG. 2. Resonant waveforms of buck-boost ZVS-QRC.

During mode 1 [t_0 t_1], the resonant capacitor voltage v_{Cr} (V_{ds} of S_1) charges linearly from 0 to $V_s + V_0$ and the inductor current i_{Lr} is maintained constant at I_m. During mode 2 [t_1 t_2], the circuit enters into resonant stage. The resonant capacitor C_r and the resonant inductor L_r resonate together. The capacitor voltage reaches the peak value of I_mZ_0, when i_{Lr} reaches zero. When the capacitor starts discharging, the inductor current has a negative value. At the end of this mode, the inductor current reaches its negative peak ($-I_m$) and the capacitor voltage drops to $V_s + V_0$. During mode 3 [t_2 t_3], the switch S_2 is turned on. The resonant capacitor voltage v_{Cr} and resonant inductor current i_{Lr} are kept constant during this mode. Switch S_2 operates under zero voltage condition, since v_{Lr} (V_{ds} of S_2) is zero during this stage. This provides inductor freewheeling, which helps in reducing switching frequency band required to regulate the output voltage. The resonant capacitor voltage discharges and reaches zero at the end of mode 4 [t_4 t_5]. As soon as v_{Cr} becomes zero, the main switch S_1 is turned on to ensure zero voltage switching. The main switch S_1 is kept on during modes 5 and 6. The inductor current i_{Lr} charges linearly and reaches I_m at the end of mode 5. The power transfer to the load takes place during modes 5 and 6. During mode 6, i_{Lr} is maintained constant at I_m and the cycle repeats.

2.2. *DC Voltage transfers gain and the control characteristics of ZVS-QRC*

The dc voltage transfer gain (M) of the converter as a function of normalized load resistance (R) and switching frequency (f_s) can be derived by equating the input energy (E_{in}) and output energy (E_0) over a complete switching cycle as

$$E_{in} = E_0. \tag{1}$$

The total input energy over one switching cycle is given by

$$E_{in} = \int_0^{T_S} i_{in} V_s dt = \int_0^{T_{d1/2}} i_{Lr} V_s dt + \int_0^{T_{d6}} i_{Lr} V_s dt \tag{2}$$

$$E_{in} = I_m V_s \left[\frac{T_{d1}}{2} + T_{d6} \right]$$

where T_{dl} and T_{d6} are the time intervals during modes 1 and 6 as shown in Fig. 2.

The output energy over one cycle is obtained by evaluating (3):

$$E_0 = \int_0^{T_S} i_0 V_0 dt = I_0 V_0 T_S. \tag{3}$$

From the conservation of energy theory, equating the input and output energy expressions to calculate the voltage transfers gain (M) of the converter, the gain M with respect to circuit parameters is given by eqn (4)

$$M = 1 - \frac{1}{\frac{f_s}{2\pi f_0}\left[\alpha + \frac{R}{2M} + \frac{M}{R}(1-\cos\alpha)\right] + \frac{2T_{d3}}{T_S}} \tag{4}$$

where T_{d3} = holding time or ON time of S_2; T_s = switching period; R_0 = load resistance;

$$\alpha = \pi + \sin^{-1}\left(\frac{V_s + V_0}{I_m Z_0}\right);\ \pi \le \alpha \le 3\pi/2. \tag{5}$$

Characteristic impedance $$Z_0 = \sqrt{\frac{L_r}{C_r}}; \tag{6}$$

Resonant angular frequency $$\omega_0 = \frac{1}{\sqrt{L_r C_r}}; \tag{7}$$

Resonant frequency $$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}; \tag{8}$$

Normalized load resistance $$R = R_0/Z_0. \tag{9}$$

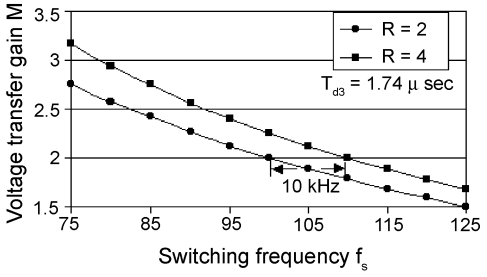

FIG. 3. Characteristics of M vs switching frequency f_s for various normalized loads ($R = R_0/Z_0$) with T_{d3} set to 1.74 microsecond.

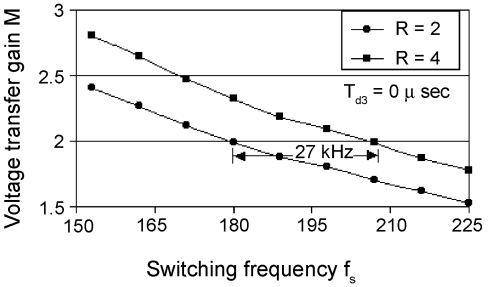

FIG. 4. Characteristics of M vs switching frequency f_s for various normalized loads ($R = R_0/Z_0$) with T_{d3} set to zero microsecond.

The value of M can be varied either by varying f_s or T_{d3}. It has been found by analysis that with the auxiliary switch S_2 set for maximum conduction time (T_{d3}), the range of switching frequency required for the control of output voltage becomes less. However, it has been increased for the same load variation when no auxiliary switch (S_2) is present in the converter. A plot of the control characteristics of M vs f_s with various normalized load (R) for two different values of T_{d3} is shown in Figs 3 and 4, respectively. It is observed that the required control range of frequency in the case of auxiliary switch control is 10 kHz compared to 27 kHz without auxiliary switch to achieve the same value of M equal to 2, when normalized load R is varied from 2 to 4.

2.3. *Design*

The design procedure of buck-boost ZVS-QRC is presented. The converter is proposed to operate in boost mode with the following parameters:

Maximum input voltage	$V_{s,\,\max} = 14$ V
Minimum input voltage	$V_{s,\,\min} = 10$ V
Output voltage	$V_0 = 24$ V
Nominal load resistance	$R_0 = 60\ \Omega$
Resonant frequency	$f_0 = 660$ kHz
Load current	$I_0 = 0$–1.2 A

(i) The range of voltage transfer gain (M)

$$M_{\min} = \frac{V_0}{V_{s,\max}} = \frac{24}{14} = 1.7; \tag{10}$$

$$M_{\max} = \frac{V_0}{V_{s,\min}} = \frac{24}{14} = 2.4. \tag{11}$$

(ii) The switching frequency (f_s) and resonant components

Based on the worst-case design (M_{max}), the switching frequency is selected as $f_s = 0.15*f_0 =$ 100 kHz. For normalized load $R = 2$, the characteristic impedance Z_0 and the resonant components L_r and C_r are calculated from eqns (6), (8) and (12).

$$Z_0 = \frac{R_0}{R} = 30\Omega. \tag{12}$$

The values of L_r and C_r are found to be 10 μH and 6 nF, respectively.

(iii) Maximum magnetizing current I_m at rated full load

$$I_m = (M_{max} + 1)I_o = 4.0 \text{ A}. \tag{13}$$

3. Design of fuzzy logic controllers

The design procedure of CFLC and SFLC for the voltage control of ZVS-QRC is presented in this section.

3.1. *Design of CFLC*

The inputs to the CFLC are the error voltage (e) and change of error voltage (ce) and the output is the change of switching frequency (Δu). Depending upon the magnitude of e and ce, the switching frequency of the main switch S_1 and auxiliary switch S_2 is varied for regulating the output voltage. The closed loop diagram of the converter with CFLC is shown in Fig. 5. The inputs to CFLC are defined as given in eqn (14) and (15).

$$e(k) = V_{ref} - V_0(k) \tag{14}$$

$$ce(k) = e(k) - e(k-1) \tag{15}$$

where V_0 is the present output voltage, V_{ref}, the reference voltage and subscript k denotes the value taken at the beginning of the k^{th} switching cycle.

The values of e, ce and Δu are normalized to a value [–1 1]. For ease of computation, the fuzzy variables e, ce and Δu are divided into five subsets using triangular function and they are labelled as PB (positive big), PS (positive small), Z (zero), NS (negative small), NB (negative big). The membership function with 50 percentage overlapping is chosen for e, ce and Δu. They are shown in Fig 6. For any combination of e and ce, a maximum of four rules are fired. For instance, if e is 0.8 and ce is –0.2, only (PS, Z), (PS, NS), (PB, Z) and (PB, NS) are fired. The inferred grades of membership for the rest of the rules are zero.

The fuzzy rule table (Table I) is established based on heuristic knowledge and results of PI controller [24]. It is observed from the PI results that for the positive error and change of error, the controller output is positive and vice versa. This helps in achieving negative feedback closed loop control and also to fix up the range of error and controller output. The rule table designed in this work is framed using this concept along with converter control characteristics. This table is stored as a look-up table containing the centroid of output fuzzy sets, while implementing in hardware. The heuristic rules used for the voltage control of buck-boost ZVS-QRC are:

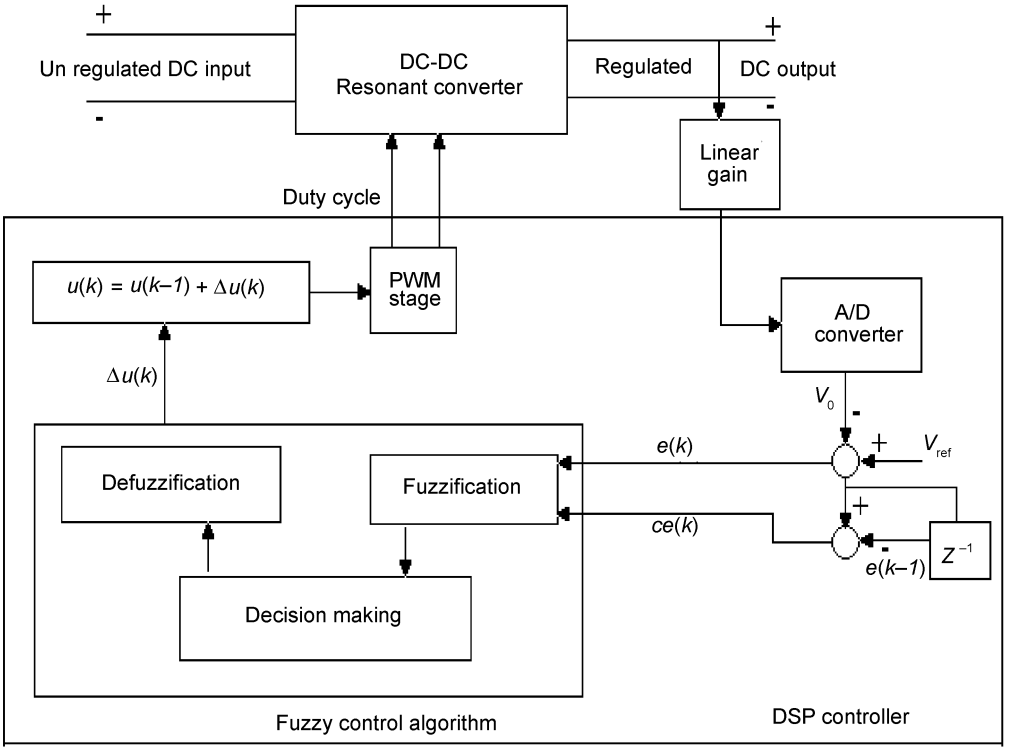

FIG. 5. Closed loop diagram of buck-boost ZVS-QRC with CFLC.

- If the output voltage is far from the reference value, then the change of switching frequency must be large so as to bring the output to the reference value quickly.
- If the output voltage approaches the reference value, then a small change of switching frequency is necessary.
- If the output voltage is near the reference value and is approaching it rapidly, then the frequency must be kept constant so as to prevent overshoot.
- If the output voltage changes even after reaching the reference value then the change of frequency must be changed by a small amount to prevent the output from moving away.

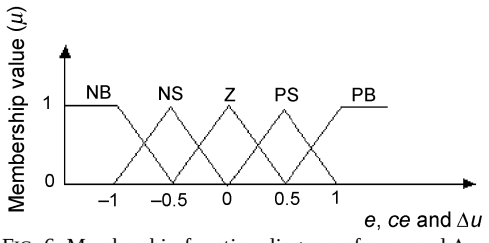

FIG. 6. Membership function diagram of *e*, *ce* and Δ*u*.

Table I
Control rules for CFLC

e/*ce*	NB	NS	Z	PS	PB
PB	Z	PS	PS	PB	PB
PS	NS	Z	PS	PS	PB
Z	NS	NS	Z	PS	PS
NS	NB	NS	NS	Z	PS
NB	NB	NB	NS	NS	Z

- If the output voltage remains constant at the reference value, then maintain the present switching frequency.

The inference result of each rule consists of two parts, the weighting factor w_i of the individual rule and the degree of change of switching frequency, C_i. The weighting factor w_i is obtained by Mamdani's minimum fuzzy implication of membership value of error (μ_e) and change of error (μ_{ce}). C_i is the centroid value of the output membership function of i^{th} rule, which is obtained from the control rule table. The inferred output of each rule can be written as

$$\Delta u_i = \min\{\mu_e, \mu_{ce}\} \bullet C_i = w_i C_i \tag{16}$$

where Δu_i denotes change of switching frequency inferred by the i^{th} rule.

After firing all the rules, the clipped outputs of the output membership function are aggregated. Applying defuzzification technique, the crisp value of switching frequency is then obtained. Many methods are used for defuzzification like the Center Of Gravity (COG), Mean of Maxima (MOM), etc. [25, 26]. Of these methods, COG method is employed in this work. The defuzzified output is change of switching frequency and is given in eqn (17).

$$\Delta u(k) = \frac{\sum_{i=1}^{N} w_i C_i}{\sum_{i=1}^{N} w_i} = \frac{\sum_{i=1}^{N} \Delta u_i}{\sum_{i=1}^{N} w_i} \tag{17}$$

where N is the maximum number of effective rules. It is seen that the calculation of eqn (17) involves multiplication and division of variables, not just the scaling of signals by constant gains. The value of the switching frequency at k^{th} instant is defined as given in eqn (18).

$$u(k) = u(k-1) + \Delta u(k). \tag{18}$$

The schematic diagram of inference mechanism of CFLC is shown in Fig. 7. The inputs of e and ce are 0.8 and –0.2, respectively. It is observed that e belongs to PS and PB, and ce to NS and Z. The four possible combinations of rules are: (i) If e is PB and ce is NS then Δu_1 is PS; (ii) If e is PB and ce is Z, then Δu_2 is PS; (iii) If e is PS and ce is NS then Δu_3 is Z; (iv) If e is PS and ce is Z, then Δu_4 is PS. For each rule, the weighting factor w_i using the minimum operation and corresponding value of C_i are calculated. Then the inferred change of switching frequency is computed using COG method as given in eqn (17). This gives Δu equal to 0.267. The effective change of switching frequency at the sampling time is therefore α time Δu. It is observed from the control characteristic as shown in Fig. 3 that for an output voltage change of ± 1.5 V with constant supply voltage there is a change in switching frequency of ± 5 kHz. Hence output denormalization factor α is taken as 5. The actual switching frequency $u(k)$ is calculated using eqn (18).

3.2. *Design of SFLC*

The SFLC is designed for CFLCs with skew symmetric property. Similar to Table I, most rule tables used in power converter applications have skew symmetric property, i.e. the out-

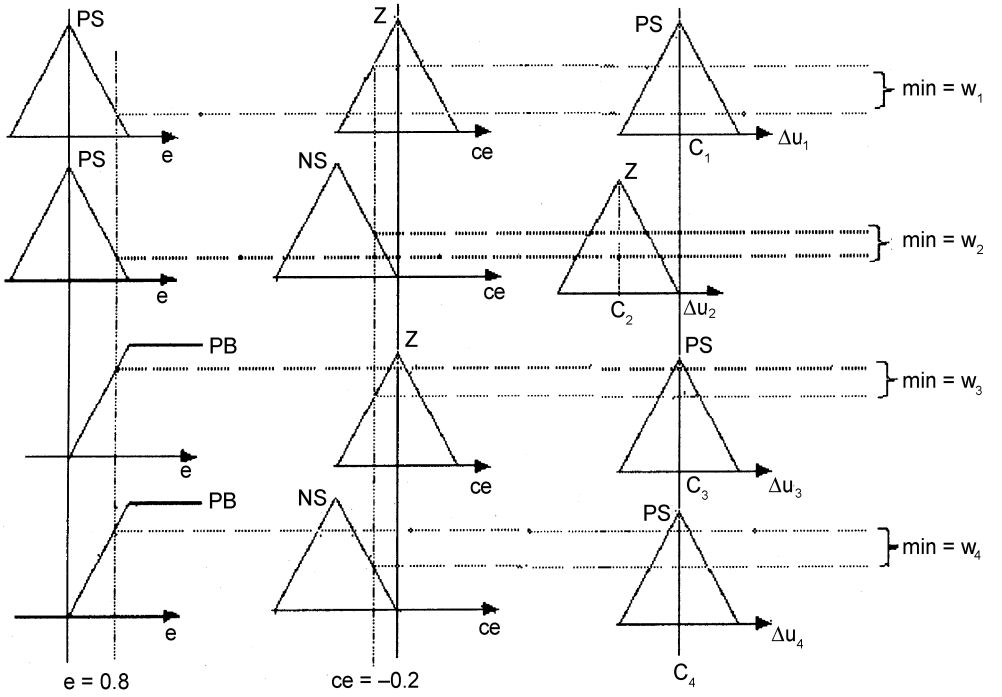

FIG. 7. Graphical illustration of inference mechanism of CFLC.

put membership function values along the leading diagonal of the rule table are zero-valued and those on either side of this diagonal take opposite signs $\Delta u_{ij} = -\Delta u_{ji}$ where Δu_{ij} is the output membership function along the i^{th} the row and j^{th} column [19, 20, 25, 26]. Also, the magnitude of the control signal is approximately equal to the distance from the main diagonal line or switching line (d_s) of the rule table as shown in Fig. 8. For a general second order system, the switching line is given in eqn (19). For the present case, switching line has unity slope passing through origin and it is defined as given in eqn (20). This property is utilized to suggest a new variable called signed distance (d_s), which is declared as the shortest distance between switching line and the present operating point. From any operating point, the control variable is directly related to the signed distance (d_s), which is the input variable to the SFLC. The output of SFLC is considered as change of switching frequency (Δu). As a result, the number of fuzzy rules required becomes minimum and the firing rule table is reduced to one-dimensional space compared to CFLC [18].

The equation for switching line is

$$ce + \lambda e = 0 \tag{19}$$

For $\lambda = 1$,

$$ce + e = 0. \tag{20}$$

The intersection point H (e, ce) of the switching line from an operating point $P(e1, ce1)$ is illustrated in Fig. 9.

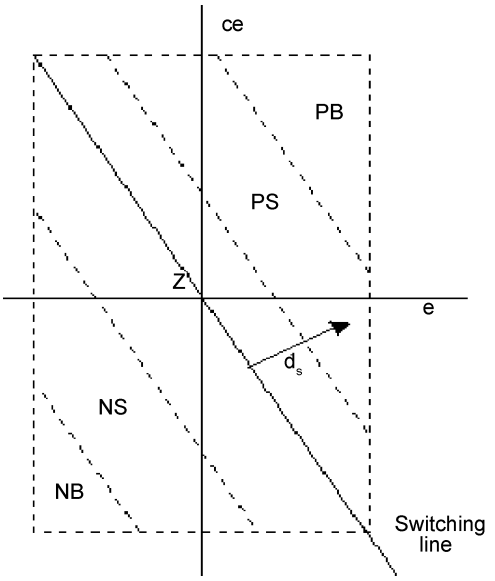

FIG. 8. Simplified plot of the CFLC rule table.

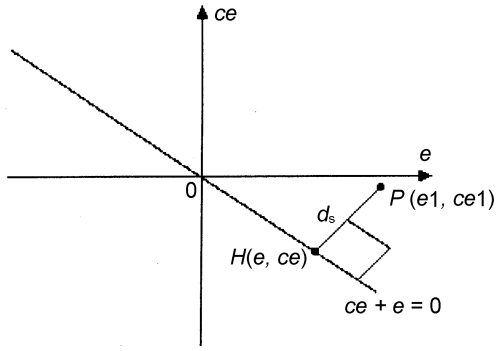

FIG. 9. Plot showing calculation of signed distance (d_s) for ZVS-QRC.

The distance d_s between $H(e, ce)$ and $P(e1, ce1)$ for a general point $P(e, ce)$ is expressed as given in eqn (21) for a second-order system and is deduced to eqn (22) for the present case.

$$d_s = \mathrm{sgn}(y) * ((|ce + \lambda e|) / \sqrt{1 + \lambda^2}); \tag{21}$$

$$d_s = \mathrm{sgn}(y) * ((|ce + e|) / \sqrt{2}); \tag{22}$$

where

$$\mathrm{sgn}(y) = \begin{cases} 1; & \text{for} \quad y > 0 \\ -1; & \text{for} \quad y < 0. \end{cases} \tag{23}$$

and

$$y = ce + e. \tag{24}$$

The sign of the control signal (Δu) for ZVS-QRC, is positive for $y > 0$ and negative for $y < 0$ and its absolute magnitude is proportional to the distance from the switching line.

Triangular membership functions with the five linguistic values are designed for d_s and Δu. The range of d_s and Δu are also normalized to [–1 1] and the membership diagram is shown in Fig. 10. The fuzzy rule for SFLC is constructed between the signed distance d_s and the control variable Δu as shown in Table II.

The inference mechanism, defuzzification and denormalization are carried out in a manner similar to CFLC.

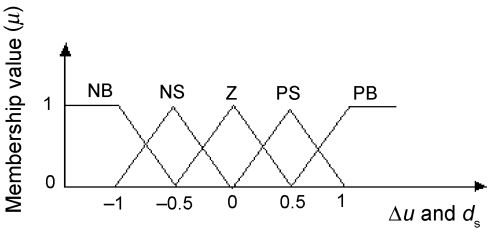

FIG. 10. Membership function diagram of d_s and Δu.

Table II
Control rules for SFLC.

d_s	PB	PS	Z	NS	NB
Δu	PB	PS	Z	NS	NB

This method can be extended to CFLC design based on n inputs. In this case, the rule table is established on n-dimensional space of e_1, e_2, …, e_n. The number of rules for m-fuzzy sets becomes m^n, which makes it very difficult to generate reasonable control rules. Similar to two-dimensional rule table, n-dimensional table also satisfies the skew-symmetric and the absolute magnitude of the control input is proportional to the distance from its main diagonal of hyper plane. The switching hyper plane is

$$e^{(n-1)} + \lambda_{n-1} e^{(n-2)} + \ldots + \lambda_2 \dot{e} + \lambda_1 e = 0. \tag{25}$$

Then signed distance D_s from the operating point to the switching hyper plane of eqn (25) can be calculated as

$$D_s = \frac{e^{(n-1)} + \lambda_{n-1} e^{(n-2)} + \ldots + \lambda_2 \dot{e} + \lambda_1 e}{\sqrt{1 + \lambda_{n-1}^2 + \ldots + \lambda_2^2 + \lambda_1^2}}. \tag{26}$$

Then the rule table is established equivalent to Table II except D_s instead of d_s. This makes SFLC very simple.

4. Simulation results

The simulated resonant waveforms of the buck-boost ZVS-QRC, shown in Fig. 11, agree closely with the theoretical waveforms shown in Fig. 2. It is observed from Fig. 11 that when v_{Cr} (V_{ds} of S_1) becomes zero, the main switch S_1 is turned on. Similarly, when V_{ds} of S_2 becomes zero, the auxiliary switch S_2 is turned on. During holding stage (t_2 to t_3) i_{Lr} is maintained constant at $-I_m$ thereby making v_{Lr} (V_{ds} of S_2) zero. This helps in reducing the switching losses.

The output voltage of converter changes with change in load disturbances. To regulate the output voltage of ZVS-QRC, a closed loop control system is designed and implemented. In closed loop operation, variable frequency control modulates the ON time of switch S_1 and OFF time of switch S_2. If the output voltage is reduced due to increased load current, the normalized switching frequency (f_{ns}) is decreased in order to increase the effective ON time and OFF time of switches S_1 and S_2, respectively. Hence, f_{ns} is inversely proportional to the power delivered to the load. This technique is used to regulate the output voltage.

Closed loop simulation using CFLC and SFLC for the voltage control of buck-boost ZVS-QRC is carried out using Matlab/Simulink software. Depending on error and the

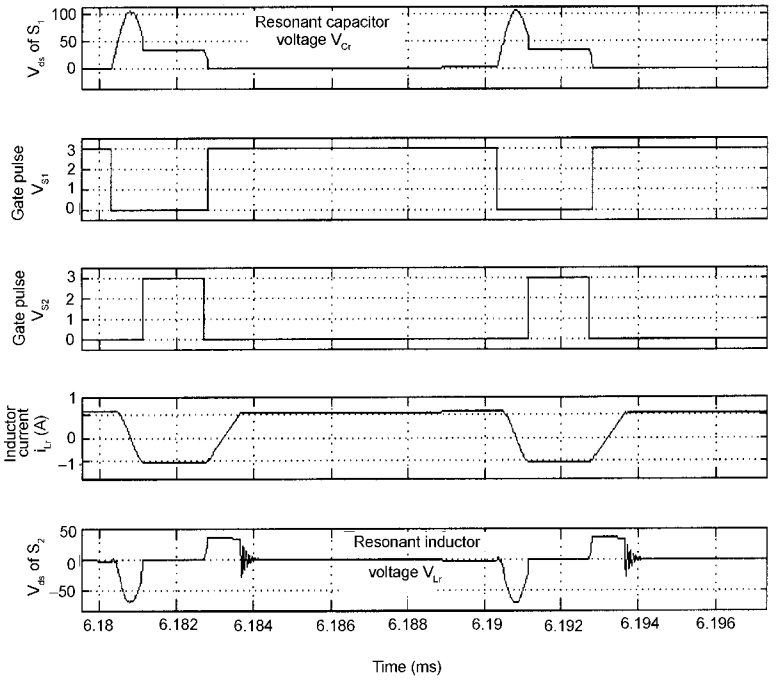

FIG. 11. Simulated resonant waveforms of buck-boost ZVS-QRC.

change of error, the value of change of switching frequency is calculated. Set parameter instruction and function blocks available in Matlab are used to update the new switching frequency of the pulse generators. The closed loop Simulink diagram of buck-boost ZVS-QRC controlled using CFLC is shown in Fig. 12. The entire system is simulated with a switching

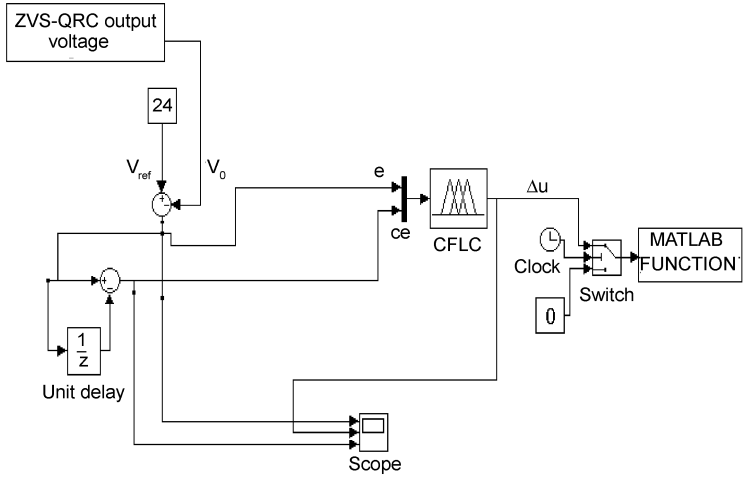

FIG. 12. Closed loop Simulink model implementing CFLC.

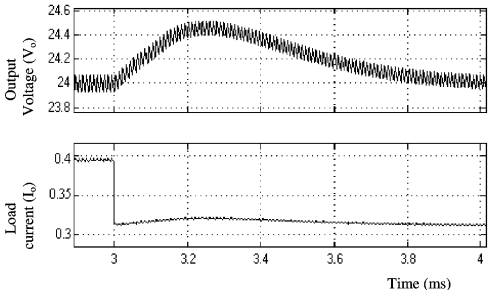

FIG. 13. Regulated output voltage and load current with CFLC for a load change from 0.4 to 0.32 A applied at 3 milliseconds.

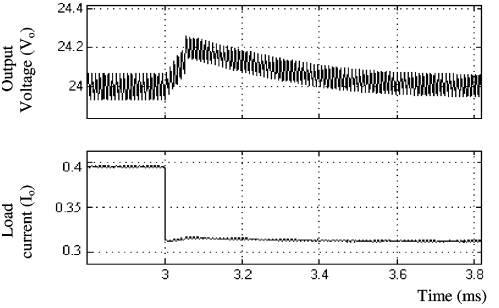

FIG. 14. Regulated output voltage and load current with SFLC for a load change from 0.4 to 0.32 A applied at 3 milliseconds.

frequency of 100 kHz. The simulated converter output voltage V_0 and load current I_0 for a step change in load from 0.4 to 0.32 A applied at 3 milliseconds is shown in Fig. 13. It is observed that the CFLC regulates the output voltage with a settling time of 0.8 millisecond.

The closed loop simulation implementing SFLC is carried out similar to CFLC with d_s as single input. The simulated converter output voltage V_0 and load current I_0 for a step change in load from 0.4 to 0.32 A applied at 3 milliseconds is shown in Fig. 14. The SFLC output is then manipulated as change of switching frequency of the pulses applied to the

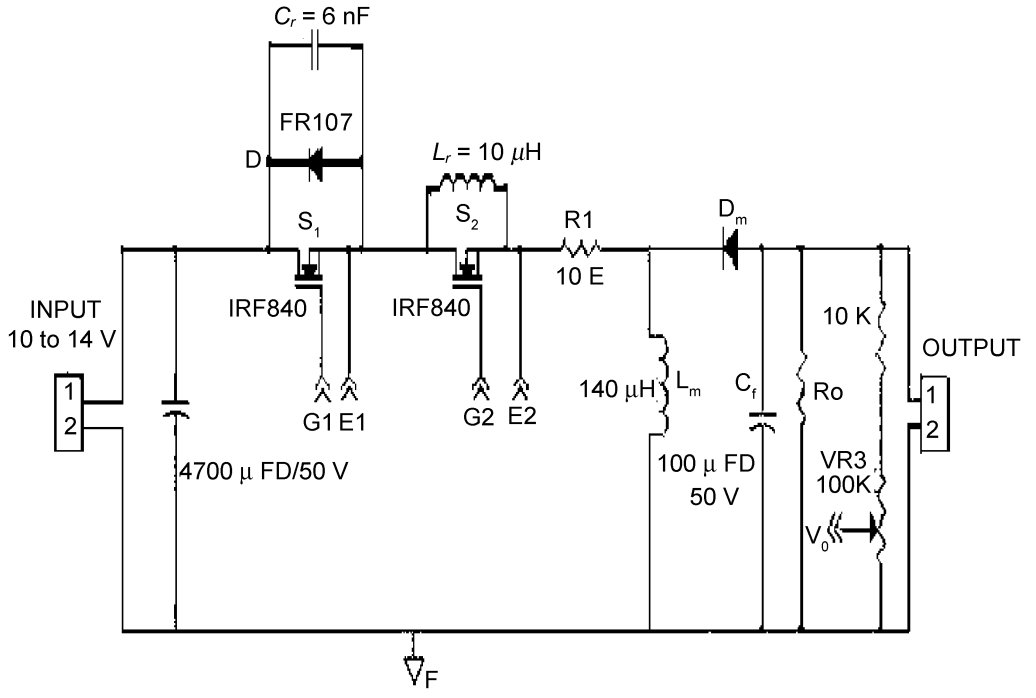

FIG. 15. Power circuit model of buck-boost ZVS-QRC.

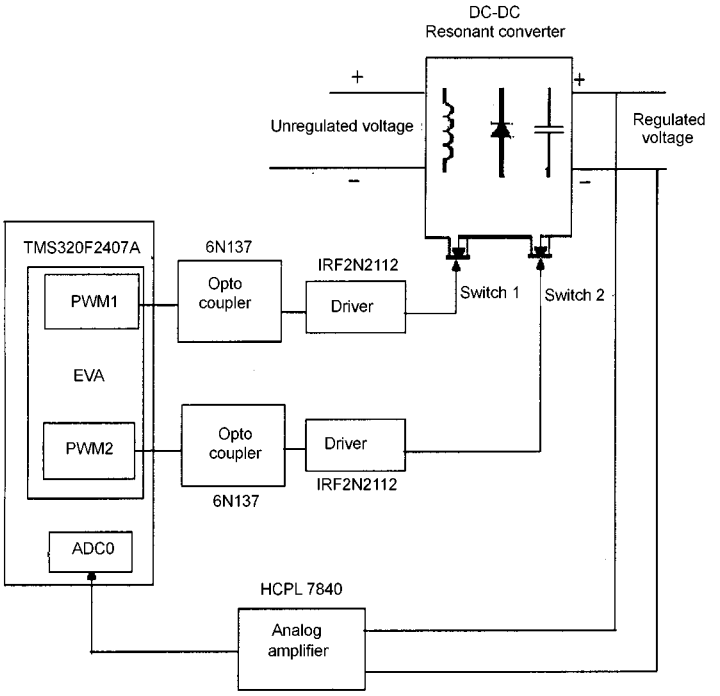

FIG. 16. Closed loop experimental set-up.

switches of ZVS-QRC. It is observed that the closed loop system regulates the output voltage with a settling time of 0.45 millisecond. Also the percentage overshoot in output voltage is reduced to 0.8% instead of 1.2% as in the case of CFLC.

5. Hardware implementation

An experimental model of buck-boost ZVS-QRC operating in boost mode is implemented with the following parameters: $V_s = 12$ V, $V_0 = 24$ V, $f_s = 100$ kHz, $L_r = 10\ \mu$H and $C_r = 6$ nF.

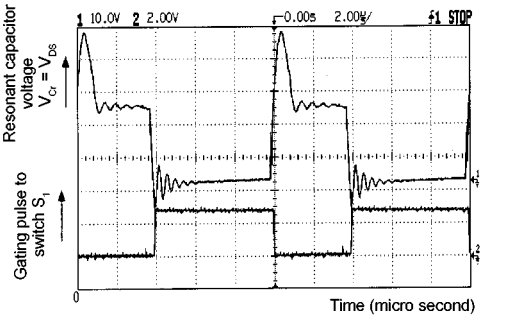

FIG. 17. Resonant capacitor voltage ($V_{Cr} = V_{DS}$) and gating pulse to switch S_1.

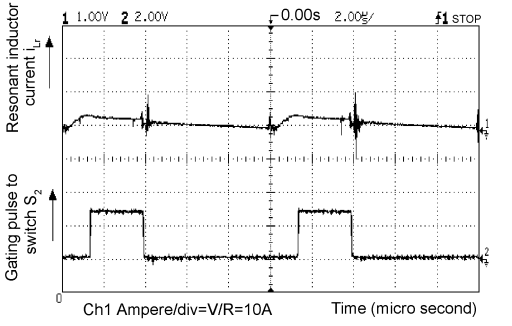

FIG. 18. Resonant inductor current (i_{Lr}) and gating pulse to switch S_2.

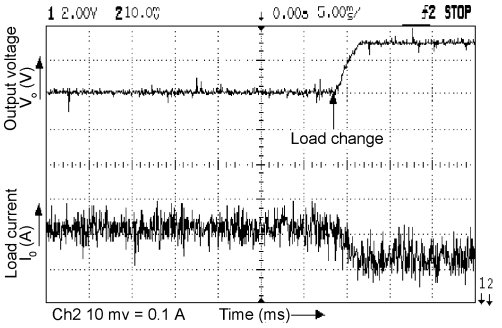

FIG. 19. Unregulated output voltage and load current for a step change in load from 0.4 to 0.32 A.

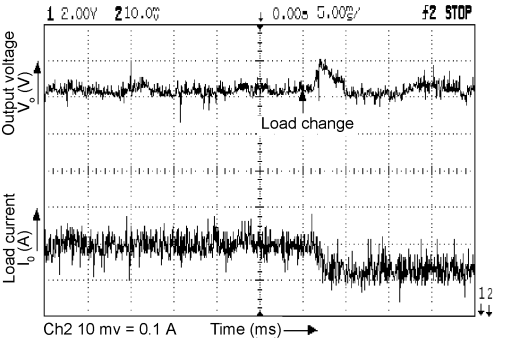

FIG. 20. Regulated output voltage and load current with CFLC for a step change in load from 0.4 to 0.32 A.

The inductors are made of ferrite core and the capacitors are of plain polyester. Power MOSFETs IRF840 are used as active switches. A fast recovery Schottky diode FR107 is used as freewheeling diode. The schematic power circuit is shown in Fig. 15. The gating pulses to switches S_1 and S_2 are generated using Event manager module (EVA), which is available in DSP processor. The pulses are applied to the gates of the MOSFET IRF840 through the opto-coupler 6N137 and driver IRF2N2112.

For closed loop operation, the converter output is sensed and scaled down to 5 V using analog amplifier HCPL 7840 (Fig. 16). The resonant capacitor voltage v_{cr} (V_{DS} of S_1) with main switch pulse V_{s1} and the resonant inductor current along with auxiliary switch pulse V_{s2}, when the converter is supplying 32% of load are shown in Figs 17 and 18, respectively. It is seen that the switches S_1 and S_2 are turned ON and OFF at nearly zero voltage condition to reduce switching losses. The experimental resonant waveforms closely agree with theoretical waveforms as shown in Fig. 2. The load current is measured using Agilent current probe with a setting of 100 mV/A.

5.1. *Experimental results with CFLC*

The unregulated output voltage for a step change in load from 0.4 to 0.32 A is shown in Fig. 19. It is observed that output voltage deviates from 24 to 27 V. The corresponding regulated output voltage implementing CFLC algorithm is shown in Fig. 20. Similarly, the unregulated output voltage for a step change in load from 0.4 to 0.5 A is shown in Fig. 21 and deviates from 24 to 22 V. The regulated output voltage implementing CFLC is shown in Fig. 22.

In closed loop operation (as shown in Figs 20 and 22), the CFLC acts effectively and forces the converter output to follow the reference value of 24 V after the load changes with settling time of 3 and 3.5 milliseconds, respectively. It takes an average of 400 instruction cycles for the 40 MHz, TMS320F2407A processor to execute the complete CFLC program, which calculates the new switching frequency for the main and auxiliary switches. The CFLC technique occupies 484 bytes of memory space for storing control algorithm.

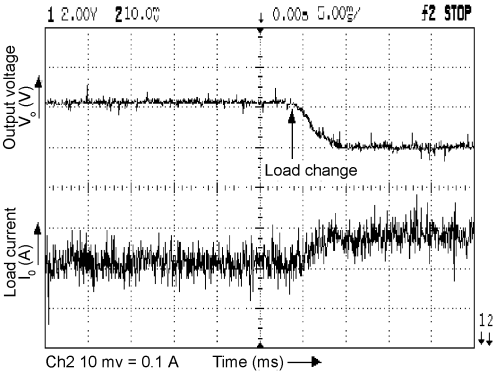

FIG. 21. Unregulated output voltage and load current for a step change in load from 0.4 to 0.5 A.

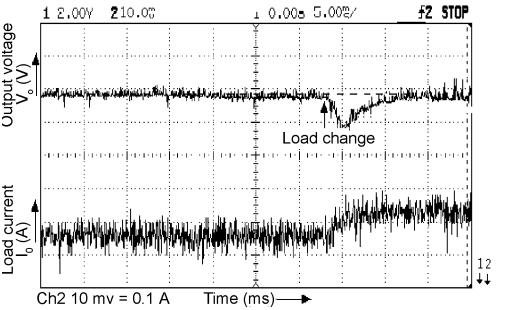

FIG. 22. Regulated output voltage and load current with CFLC for a load change from 0.4 to 0.50 A.

5.2. *Experimental results with SFLC*

The number of rules required for the proposed SFLC is five. This makes the algorithm powerful when compared to CFLC. The voltage regulation of the converter with SFLC for the same load changes applied as in CFLC method are shown in Figs 23 and 24, respectively. It is seen that, the output voltage is regulated after the load changes with settling time of 1 and 2 milliseconds, respectively. The new switching frequency obtained by SFLC is updated approximately every switching cycle.

For this application, SFLC reduces considerably the instruction cycles required from 400 to 240 and memory space from 484 to 213 bytes when compared to CFLC. Hence, it is amenable for implementation in DSP processors. Due to reduced execution time, SFLC has the ability to regulate the output voltage against load disturbances faster than CFLC thereby reducing the settling time.

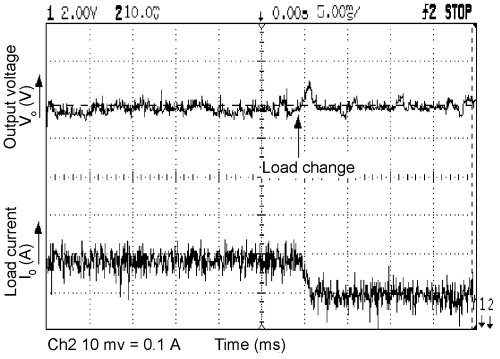

FIG. 23. Regulated output voltage and load current with SFLC for a step change in load change from 0.4 to 0.32 A.

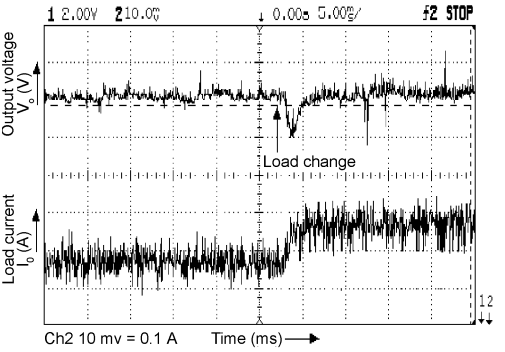

FIG. 24. Regulated output voltage and load current with SFLC for a load change from 0.4 to 0.5 A.

Table III
Performance measures of ZVS-QRC using CFLC and SFLC

Controllers	Simulation studies for load variation from 0.4 to 0.32 A		Experimental studies for load variation from 0.4 to 0.32 A				
	Percentage overshoot	Settling time (ms)	Percentage overshoot	Settling time (ms)	Execution time (μs)	Number of rules required	Memory required for storing control algorithm (bytes)
CFLC	1.8	0.8	4.1	3	10	25	484
SFLC	0.8	0.45	2.1	1	6	5	213

6. Conclusion

The design and implementation of SFLC for the closed loop voltage regulation of buck-boost ZVS-QRC is discussed in this paper. The derivation of the SFLC algorithm is presented. The effectiveness of SFLC as compared with CFLC is verified by simulation and experimental studies. It is proved from the performance table (Table III) that the execution time and memory space are greatly reduced when compared to CFLC. Also it improves the transient performance. This switched mode power supply is designed for low power applications. The SFLC algorithm can be effectively implemented for other converter topologies or complex structured nonlinear systems controlled using microcontroller or DSP processor.

References

1. K. H. Liu, and F. C. Y. Lee, Zero voltage switching technique in dc-dc converters, *IEEE Specialists Conf. Rec.*, 58–70 (1986).
2. Ivo Barbi, J. C. Bolacell, D. C. Martins, and F. B. Libano, Buck quasi-resonant converter operating at constant frequency: Analysis, design and experimentation, *IEEE,* 873–880 (1989).
3. S. Arulselvi, G. Uma, and M. Chidambaram, Design of PID controller for boost converter with RHS zero, *IEEE-4th Int. Conf. on Power Electronics and Motion Control,* Xi'an University, China, pp. 532–537 (2004).
4. G. Uma, M. Shanthi, and C. Chellamuthu, Design and implementation of constant frequency soft-switched regulated power supply for aerospace applications, *IEEE-ISIE'2000,* Cholula, Puebla, Mexico (2000).
5. C. Namuduri, and P. C. Sen, A servo-control system using a self-controlled synchronous motor with sliding mode controller, *IEEE Trans. Ind. Applic.*, **23**, 283–285 (1987).
6. R. Venkataramanan, A. Sabanovic, and S. Cuk, Sliding mode control of dc-dc converters, *IEEE-IECON Rec*., pp. 251–258 (1985).
7. P. Mattavelli, L. Rossetto, G. Spiazzi, and P. Tenti, General-purpose fuzzy logic controller for dc-dc converters, *IEEE Trans. Power Electronics,* **12**, 79–86 (1997).
8. B. K. Bose, Expert system, fuzzy logic and neural network applications in power electronics and motion control, *Proc. IEEE,* **82**, 1303–1323 (1994).
9. A. Balestroni, A. Landi, and L. Sani, Cuk converter global control via fuzzy logic and scaling factors, *IEEE Trans. Ind. Applic.,* **147**, 107–112 (2000).
10. K. Viswanathan, R. Oruganti, and D. Srinivasan, A universal fuzzy controller for a nonlinear power converter, *FUZZ-IEEE'02 Conf. Rec*., pp. 46–51 (2002).
11. Yigang Shi, and P. C. Sen, A new defuzzification method for fuzzy control of power converters, *IEEE,* pp. 1202–1209 (2000).
12. Yigangi Shi, and P. C. Sen, Application of variable structure fuzzy logic controller for dc-dc converter, *IECON'01: The 27th Annual Conf. of the IEEE Industrial Electronic Society,* pp. 2026–2031 (2001).

13. B. R. Lin, Analysis of neural and fuzzy power electronic control, *IEE Proc. Sci. Meas. Technol.*, **144**, 25–31 (1997).
14. G. Uma, J. Latha and C. Chellamuthu, A fuzzy speed controller for soft switched dc-dc converter fed DC servomotor for aerospace applications, *IEEE-ISIE'2000*, Cholula, Puebla, Mexico, pp. 730–734 (2000).
15. V. S. C. Raviraj, and P. C. Sen, Comparative study of proportional-integral, sliding mode, and fuzzy logic controllers for power converters, *IEEE Trans. Ind. Applic.*, **33**, 518–525 (1997).
16. Wing-Chiso, Chi K. Tse, and Yim-Shu Lee, Development of a fuzzy logic controller for dc-dc converters: Design, computer simulation and experimental evaluation, *IEEE Trans. on Power Electronics*, **11**, 24–31 (1996).
17. Tarun Gupta, R. R. Boudreaux, R. M. Nelms, and John Y. Hung, Implementation of a fuzzy controller for dc-dc converters using an inexpensive 8-b microcontroller, *IEEE Trans. Ind. Electronics*, **44**, 661–669 (1997).
18. Byung-Jae Choi, Seong-Woo Kwak, and Byung Kook Kim, Design and stability analysis of single input fuzzy logic controller, *IEEE Trans. Systems, Man, Cybernetics: Part b Cybernetics*, **30**, 303–309 (2000).
19. K. Viswanathan, R. Oruganti, and D. Srinivasan, Nonlinear function controller: A simple alternative to fuzzy logic controller for a power electronic converter, *IEEE Trans. Ind. Electronics*, **52**, 1439–1448 (2005).
20. K. Viswanathan, R. Oruganti, and D. Srinivasan, Design and analysis of SISO fuzzy logic controller for power electronic converters, *FUZZ-IEEE :IEEE Int. Conf. of Fuzzy Systems*, Hungary, pp. 1293–1298 (2004).
21. S. Arulselvi, G. Uma, L. Hemuchandiran, and V. Saminath, Design and implementation of simple fuzzy logic controller (SFLC) for the voltage control of resonant converters, *IEEE APEC*, Austin, pp. 1508–1514 (2005).
22. P. Dananjayan, and C. Chellamuthu, A constant frequency zero voltage switching quasi-resonant converter for aerospace applications, *Int. J. Electronics*, **83**, 397–416 (1997).
23. S. Arulselvi, T. Archana, and G. Uma, Design and implementation of constant frequency zero voltage switching quasi-resonant controller UC3861 for aerospace applications, *IEEE Int. Conf. on Power System Technology*, Singapore, pp. 1270–1275 (2004).
24. S. Arulselvi, A. Biju, and G. Uma, Design and simulation of fuzzy logic controller for a constant frequency quasi–resonant dc-dc converter, *IEEE Int. Conf. on Intelligent Sensing and Information Processing*, Chennai, India, pp. 472–476 (2004).
25. D. Driankov, H. Hellendoorn, and M. Reinfrank, *An introduction to fuzzy control*, Narosa Publishing House, New Delhi, India (1993).
26. Ronald R. Yager and Dimitar P. Filev, *Essentials of fuzzy modeling and control*, Wiley, pp. 282–311 (2002).

Nomenclature with units

V_s	Input voltage (V)
V_0	Output voltage (V)
i_{Lr}	Resonant inductor current (A)
v_{Cr}	Resonant capacitor voltage (V)
I_m	Magnetizing current (A)
R_0	Load resistance (ohm)
M	Voltage transfers gain
Z_0	Characteristic impedance (ohm)
I_0	Load current (A)
f_0	Resonant frequency (kHz)
f_s	Switching frequency (kHz)
f_{ns}	Normalized switching frequency
R	Normalized load
v_{Lr}	Resonant inductor voltage (V)