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A smart power ASIC (SPIC) for a distributed power system

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Abstract

We describe the design and implementation and discrete validation of a high-voltage BCD-technology-based smart power integrated circuit (SPIC) design, which is an 'one-chip solution' to control, drive, and protect a two-stage distributed power system (DPS). As such, the proposed SPIC achieves higher power density, reduced design-cycle time, and enhanced system reliability. DPS comprises a front-end ac/dc single-switch power factor-correction (PFC) converter, which is cascaded with a back-end dc/dc four-switch full-bridge zero-voltage switching (FBZVS) converter. The current- and the voltage-mode controllers for the PFC and the FBZVS converters, respectively, are integrated into the SPIC. The SPIC can 'directly' fire the two high-side and three low-side devices in the power system. A combination of bootstrap and charge-pump techniques is used to power the gate drive circuits for the high-side power devices; hence, the duty cycle for a high-side power device is 100% and independent of the turn-on time of the low-side power device in the same leg of the FBZVS converter. Additionally, a more reliable two-stage fault protection scheme is implemented in the SPIC including protection features such as under-voltage lockout, over-current protection, adaptive shoot-through protection, and soft-start capability. This paper illustrates several key experimental results obtained by controlling DPS using the discrete SPIC to validate the functionalities of the latter and the satisfactory performance of the overall system.

Keywords: Smart power integrated circuit, power factor correction, dc/dc converter, full bridge, zero-voltage switching, and distributed power system.

1. Introduction

The architectures of power-electronics systems are becoming increasingly complex with a gradual transition from standalone single-module systems to multi-module distributed power systems (DPSs). Inevitably, this leads to higher design-cycle time, which needs to be reduced. Conventionally, a controller board for a power supply consists of the control, gate-drive, and fault-protection circuits implemented with 'discrete' components. However, to keep pace with the need for reduced package sizes and parts count and increased power densities, it is essential to pursue an integrated systems approach to standardize power-electronics components and packaging techniques in the form of an integrated power electronics module (IPEM) [1]. Towards this end, an additional necessity is to operate power converters at progressively higher switching frequencies. To minimize the effects of parasitics at high switching frequencies, it is necessary to reduce the trace lengths of printed-

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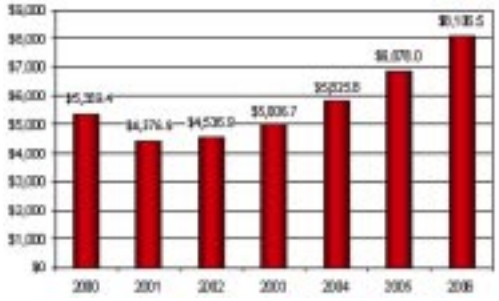
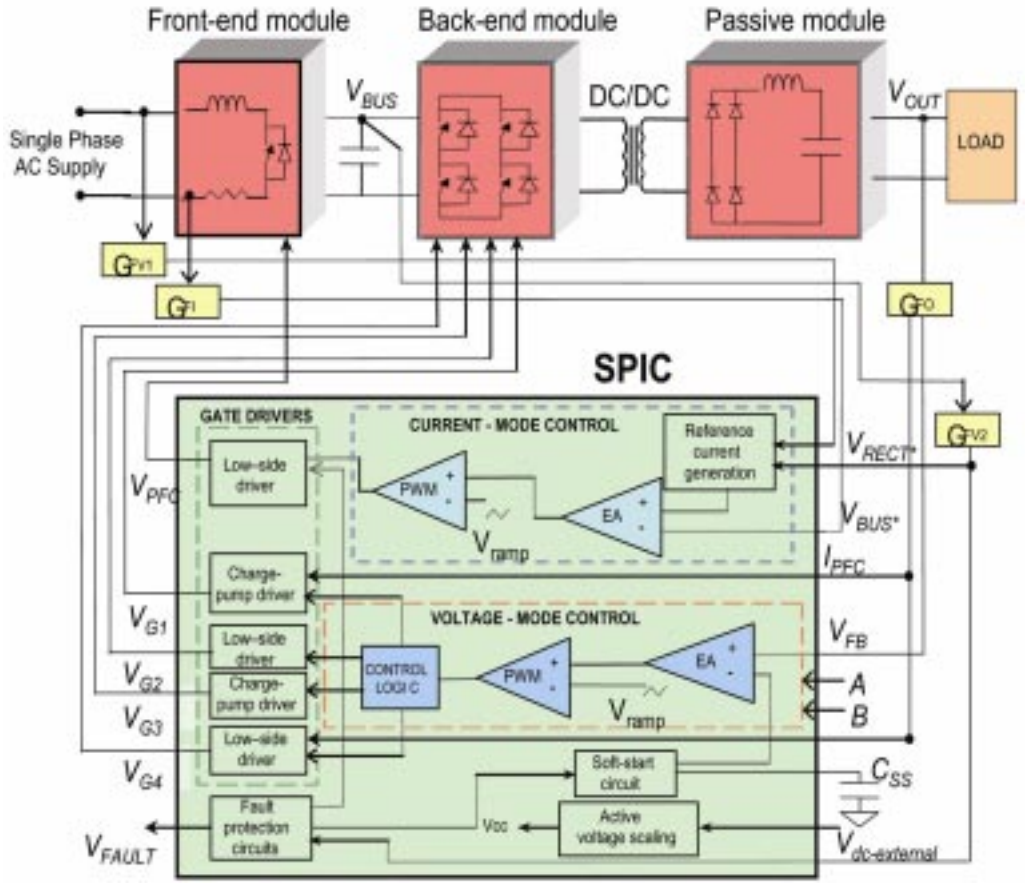


FIG. 1. Global shipment forecast for power-management ICs.

circuit boards (PCBs). However, thin copper traces increase the overall resistance of a PCB and makes it even more difficult to maintain adequate power supply regulation at all points of load on a PCB.

The rapid advancement in VLSI has provided an avenue for meeting these demanding industry requirements. Today, a large per cent of circuits in electronic systems are implemented with integrated circuits (ICs). The family of integrated circuits dedicated towards the design of power conditioning systems is known as power-management ICs [2–4]. Using such power-management ICs, the business projection of which is shown in Fig. 1, it is now possible to integrate a complete controller in a single chip, which is evident from the recently released power-factor controller IC TDA 4862 from Siemens [5]. The gate-drive circuits for power devices can also be integrated within a chip. The ISL 6520 controller IC from Intersil [6] incorporates the gate-drive circuits for a synchronous buck converter. By extending this concept to full-bridge converter modules, Intersil developed the HIP 408X family of H-bridge driver ICs [7], which are capable of driving two high-side power devices. On a similar note, significant improvements in cost and performance can be achieved if the control and drive stages of a DPS are integrated. For instance, International Rectifier released the IR2167 [8], which controls a two-stage ballast system. The IC integrates the control and drive circuits for a PFC and half-bridge converter module.

As a further development, we propose a ‘one-chip’ controller-driver solution for a DPS comprising a single-switch ac/dc power-factor-correction (PFC) converter cascaded with a dc/dc full-bridge zero-voltage switching (FBZVS) converter [9–11]. The current and the voltage-mode controllers for the PFC and the FBZVS converters, respectively, along with a more reliable two-stage fault protection scheme, are integrated in a single smart power integrated circuit (SPIC). SPIC incorporates protection features such as under-voltage lockout, over-current protection, adaptive shoot-through protection, and a soft-start capability. The chip directly fires two high-side and three low-side devices of the PFC-FBZVS DPS. A combination of bootstrap and charge-pump techniques is used to power the high-side gate-drivers and hence, the maximum duty cycle (of 100%) for a high-side device in one leg of the full-bridge is independent of the turn-on time of the low-side device in the same leg. SPIC is designed using a high-voltage BCD technology, which permits the integration of control sections and power devices on the same chip. The control circuit, which is implemented using low-voltage CMOS devices, has a low static power consumption, high noise margin, low cost, and high integration density, while the power device is implemented



EA	–	Error amplifier	G_{FI}	–	Current sensor gain
PWM	–	Pulse width modulator	G_{FV1}, G_{FV2}, G_{FO}	–	Voltage sensor gains
V_{RECT*}	–	Scaled version of the rectified source voltage	$V_{G1\text{-}4}$	–	Gate-drive signals for the full-bridge module
			V_{PFC}	–	Gate drive signal for the front-end module
V_{BUS*}	–	Scaled bus voltage	$V_{dc\text{-}external}$	–	External power supply
V_{FB}	–	Scaled output voltage	A, B	–	Externally programmable dead-time inputs
I_{PFC}	–	Scaled inductor current			

FIG. 2. Block diagram of the DPS. It shows the PFC and the FBZVS converters, both of which are controlled by SPIC.

using an LDMOS due to their compatibility with low-voltage devices [4]. The bipolar section is used for gate-drivers due to their higher current driving capability. System-level simulations are performed using the Cadence Design II Framework which enables a co-simulation of the power stage (in Saber Designer) and SPIC models (Cadence) on a common platform. The complete power system is implemented on a PCB and controlled using a discrete controller-driver implementation of the proposed SPIC. The experimental results show excellent steady-state and transient performances.

2. SPIC design

The functional block diagram for SPIC along with DPS is shown in Fig. 2. The complete design and operational details of the DPS comprising an ac/dc PFC converter (front-end module) followed by a dc/dc FBZVS converter (Back-end module) and SPIC are described in [12]. Here, we describe the salient design aspects of SPIC.

2.1. *Controller design*

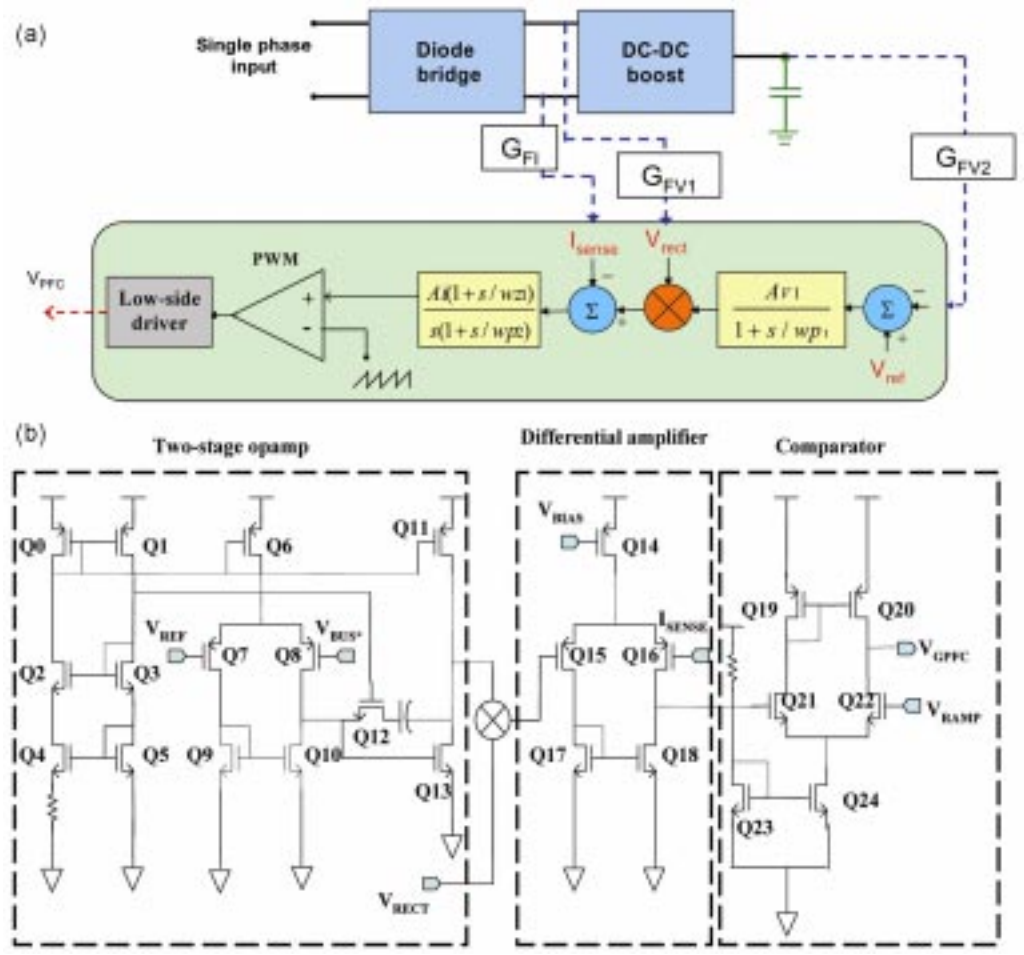
The control structure for the PFC converter (shown in Fig. 3(a)) is implemented using two loops [13]: a low bandwidth outer voltage loop that regulates the output voltage at 48 V and a high bandwidth inner current loop operating using average current-mode control [12, 14–17]. The latter, shapes the input ac current to be drawn sinusoidally from the single-phase ac source in synchronism with the input voltage [9], thereby minimizing the harmonics of the input current. To generate this sinusoidal current reference, the output outer voltage-loop controller is multiplied with the rectifier input voltage (VRECT). The compensation pole for the voltage controller (with a dc gain of A_{v1}) is placed at 15 Hz to filter the 120 Hz ripple in the bus voltage, thereby achieving low distortion in the inductor current. The inner current loop is comparatively very fast in order to track current changes. A simple PI controller with a large proportional is used to design the current compensator [13]. The compensation pole ω_{p2} for the inner current controller is placed near half the switching frequency, while the compensation zero ω_{Z2} and dc gain A_i are tuned to optimize the controller bandwidth. The output of the inner current controller is compared with a high-frequency ramp to create the PWM signal, which is subsequently level-shifted to fire the PFC switch.

The transistor-level realization of the PFC controller [13] is shown in Fig. 3(b). It comprises a differential amplifier at the input stage which functions as the outer voltage-loop controller. The output from this stage is fed to an analog multiplier which generates the current reference for the inner current loop. The current-mode controller calculates the error between this reference signal and the inductor current (I_{SENSE}). The output signal from the high bandwidth current-mode controller is the duty ratio and is compared with a 0–3 V ramp signal (V_{RAMP}) fed at the inverting terminal of the PWM modulator. The PWM modulator is implemented using a high-gain differential amplifier. VBIAS and VREF are internally derived reference signals, while VGPFC is fed to the low-side gate driver. The layouts of the two-stage opamp and comparator are shown in Figs 4(a) and (b), respectively [13].

The analog multiplier, which generates the reference current for the inner current loop, is implemented using a voltage-controlled variable linear resistor comprising two transistors in the feedback network of an opamp as shown in Fig. 5 [18, 19]. The voltage-conversion ratio of an opamp in a non-inverting configuration is given by

$$A_v = 1 + \frac{R_f}{X_1},$$

where X_1 is the effective input impedance ($r_{dsMR1}//r_{dsMR2}$). Using first-order approximations, it has been shown in [20] that the equivalent resistance of the variable linear resistor is given by



$(W/L)_{Q0}$ = 25/1.6	$(W/L)_{Q5}$ = 25/1.6	$(W/L)_{Q10}$ = 150/1.6	$(W/L)_{Q15}$ = 300/1.6	$(W/L)_{Q20}$ = 150/1.6
$(W/L)_{Q1}$ = 25/1.6	W/L)$_{Q6}$ = 300/1.6	$(W/L)_{Q11}$ = 300/1.6	$(W/L)_{Q16}$ = 300/1.6	W/L)$_{Q21}$ = 150/1.6
$(W/L)_{Q2}$ = 25/1.6	$(W/L)_{Q7}$ = 300/1.6	$(W/L)_{Q12}$ = 100/1.6	$(W/L)_{Q17}$ = 150/1.6	$(W/L)_{Q22}$ = 50/1.6
$(W/L)_{Q3}$ = 25/1.6	$(W/L)_{Q8}$ = 300/1.6	$(W/L)_{Q13}$ = 300/1.6	$(W/L)_{Q18}$ = 150/1.6	$(W/L)_{Q23}$ = 100/1.6
$(W/L)_{Q4}$ = 100/1.6	$(W/L)_{Q9}$ = 150/1.6	$(W/L)_{Q14}$ = 300/1.6	$(W/L)_{Q19}$ = 50/1.6	$(W/L)_{Q24}$ = 150/1.6

Model parameters for nmos24

vto	0.775	tox	400e-10	nsub	8e15	xj	0.15e-6	ld	0.2e-6
uo	650	ucrit	0.62e5	pb	0.8	cgso	1.95e-10	cj	195e-6

Model parameters for pmos24

vto	–0.775	tox	400e-10	nsub	8e15	xj	0.15e-6	ld	0.2e-6
uo	650	ucrit	0.62e5	pb	0.8	cgso	1.95e-10	cj	195e-6

FIG. 3. (a) Controller architecture of the ac/dc PFC converter, and (b) transistor-level implementation of the PFC controller.

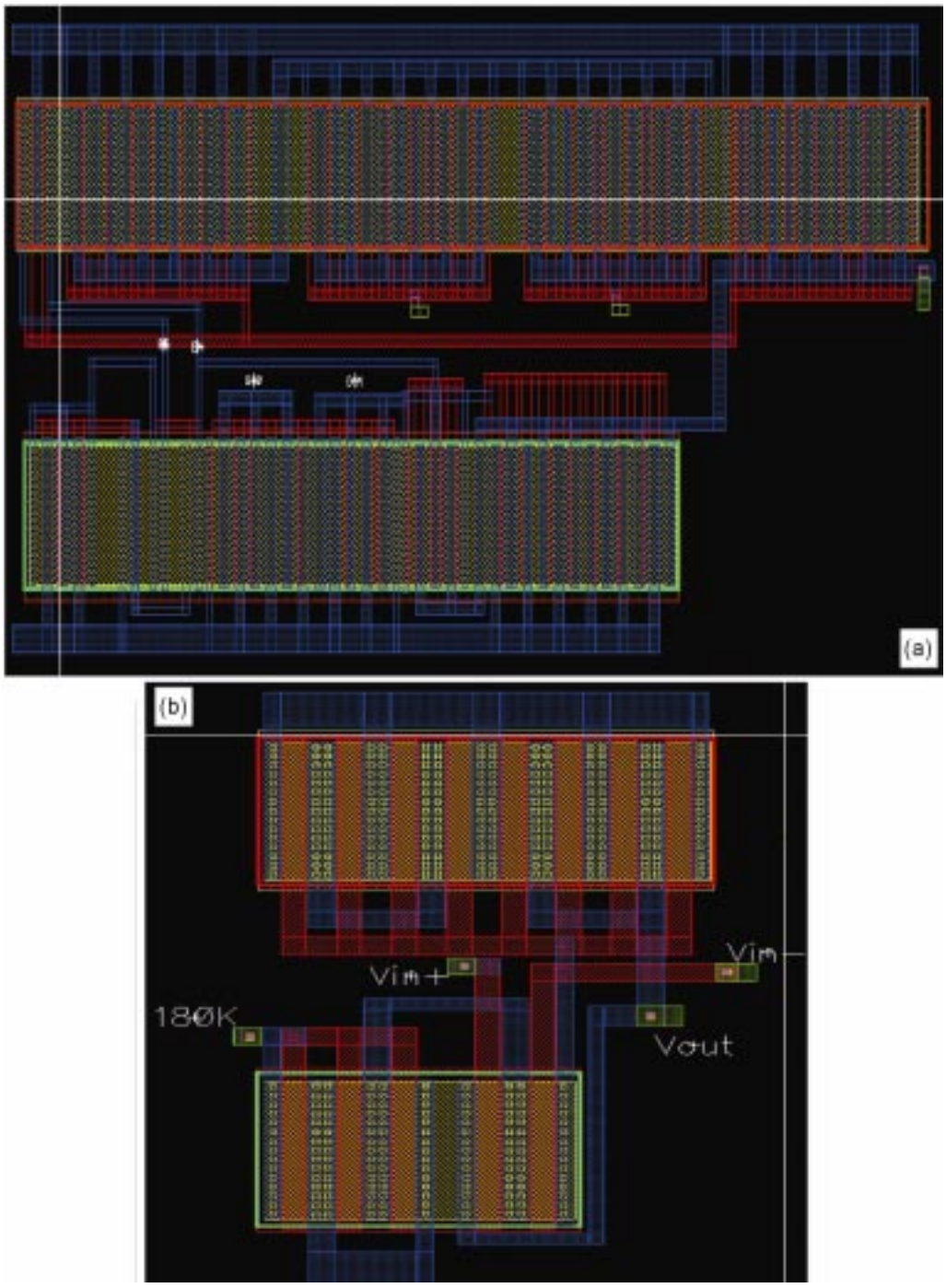


FIG. 4. Layouts of (a) the opamp, and (b) the comparator.

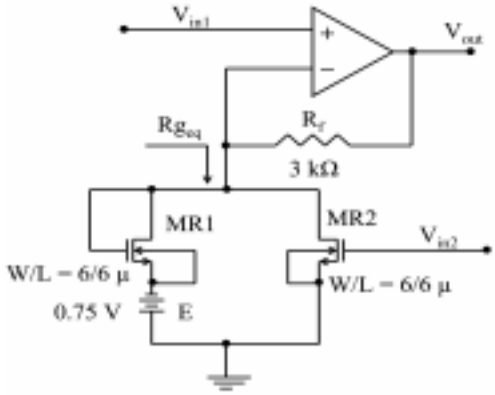


FIG. 5. Analog multiplier based on non-inverting opamp.

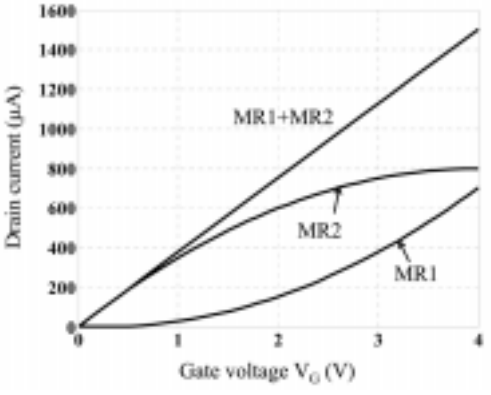


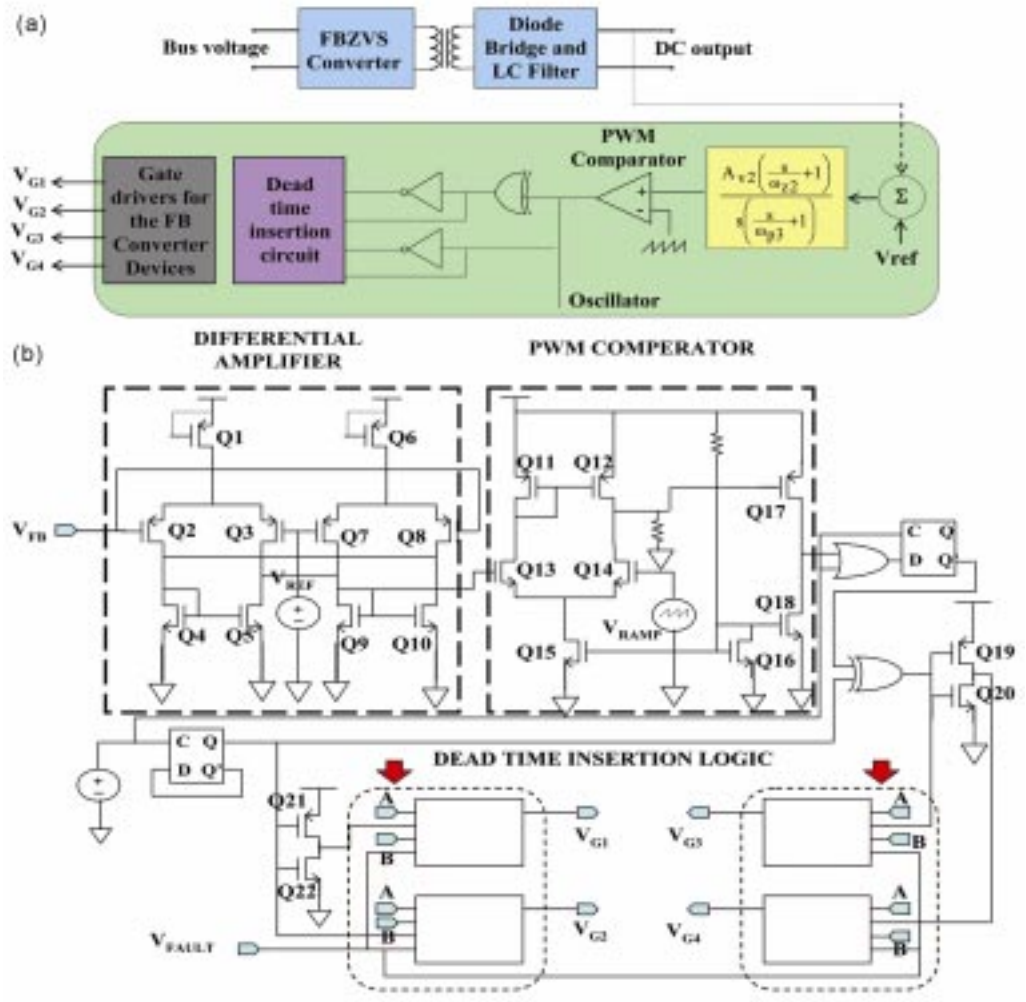
FIG. 6. I–V characteristics of the FETs that comprise the variable linear resistor.

$$Rg_{eq} = \frac{1}{[K(V_{in2} - 2V_T + E)]},$$

where, $K = \mu_0 C_{ox} W_{MR1}/L_{MR1}$, μ_0 is the surface mobility of the channel for the MOS device, C_{ox}, the capacitance per unit area of the gate oxide, and E, the bias offset voltage. The I–V characteristics of the two transistors (MR_1 and MR_2) are shown in Fig. 6. Hence, by varying the conductance $\mathbf{r}_{dsMR2}$ of MR_2 via a control signal (i.e. output of the voltage mode controller) at its gate, the effective impedance (X1) is modulated to create a multiplier. However, this is only true when $V_{in1} \leq (V_{in2} - V_T)$ in order to keep M_{R2} in its linear region. Furthermore, M_{R1} is always operating in the saturation region because $V_{DS1} \geq (V_{GS1} - V_T)$.

The front-end PFC module is cascaded with the FBZVS converter using an intermediate dc bus capacitor. Constant-frequency voltage-mode PWM control is employed to regulate the output voltage at 48 V. This is achieved by turning on each switch in each leg of the FBZVS converter for 50% of the switching cycle, while the effective duty ratio is determined by the phase shift between the two legs of the bridge [9]. A two-pole single-zero compensator is used to regulate the output of the FBZVS at 48 V. The realization of this compensator and its transfer function is shown in Fig. 7(a). A high-frequency oscillator is used to generate the gate pulses for one leg of the bridge while the pulses for the second leg are generated by XOR-ing the output of the PWM modulator and the oscillator. The four PWM signals are then fed through dead-time insertion circuits that prevent the simultaneous turn on of two power devices in the same leg of the bridge. The output from this stage is then fed through the gate-driver circuits for the four power devices.

The complete transistor-level realization of the FBZVS is shown in Fig. 7(b). We use standard dimensions for all the digital gates used in the design of SPIC, i.e. (for an *n*-channel enhancement-mode mos–W/L = 0.5 μ/0.5μ, while for a *p*-channel enhancement-mode mos–W/L = 1.5/0.5μ). We use a 100 kHz oscillator to generate the gate pulses for one leg of the bridge. The PWM signals for the other leg are generated by XOR-ing the output of the PWM comparator and the 100 kHz oscillator. The gate-control signals for the four



$(W/L)_{Q1}$ = 300/1.6	$(W/L)_{Q6}$ = 300/1.6	$(W/L)_{Q11}$ = 150/1.6	$(W/L)_{Q16}$ = 150/1.6	$(W/L)_{Q21}$ = 300/1.6
$(W/L)_{Q2}$ = 300/1.6	$(W/L)_{Q7}$ = 300/1.6	$(W/L)_{Q12}$ = 150/1.6	$(W/L)_{Q17}$ = 300/1.6	$(W/L)_{Q22}$ = 300/1.6
$(W/L)_{Q3}$ = 300/1.6	$(W/L)_{Q8}$ = 300/1.6	$(W/L)_{Q13}$ = 150/1.6	$(W/L)_{Q18}$ = 300/1.6	
$(W/L)_{Q4}$ = 150/1.6	$(W/L)_{Q9}$ = 150/1.6	$(W/L)_{Q14}$ = 150/1.6	$(W/L)_{Q19}$ = 300/1.6	
$(W/L)_{Q5}$ = 150/1.6	$(W/L)_{Q10}$ = 150/1.6	$(W/L)_{Q15}$ = 100/1.6	$(W/L)_{Q20}$ = 300/1.6	

FIG. 7. (a) Control structure of the FBZVS converter, and (b) transistor-level implementation of the FB controller.

power devices are then fed through a signal-conditioning stage (dead-time generation for ZVS and preventing overlap between the two switches of the same leg of the bridge) before being fed to their respective gate-driver circuits. V_{FAULT} in Fig. 7(b) is generated by the fault-protection block while VFB is the scaled down output voltage of DPS. When a fault is detected, the power devices are protected by disabling their gate control signals (V_{G1}–V_{G4}).

Table I
Model parameters for high-voltage Philips DMOS

Model parameters for Philips nmos3002							
ron	1	tox	1.e-5	cgate	1.e-12	af	1.0
rsat	100	+ dch	1e16	+ csub	5.e-13	tref	25
vsat	20.0	dsub	1.e15	tausc	1.e-12	+ dta	0.0
psat	1.0	vsub	0.6	ach	1.0	mult	1.0
vp	0.5	vgap	1.206	kf	0.0		
Model parameters for Philips pmos3002							
ron	1	tox	1.e-5	cgate	1.e-12	af	1.0
rsat	100	+ dch	1e16	+ csub	5.e-13	tref	25
vsat	20.0	dsub	1.e15	tausc	1.e-12	+ dta	0.0
psat	1.0	vsub	0.6	ach	1.0	mult	1.0
vp	–0.5	vgap	1.206	kf	0.0		

The mechanism by which ZVS is achieved is different for both legs of the bridge. In order to ensure that Q4 turns ON with almost zero voltage across it, a dead time is needed between the turn OFF of Q2 and turn ON of Q4 to ensure that D4 conducts prior to turn ON of Q4. Hence, this dead time is calculated to ensure the maximum possible load range to achieve ZVS. The resonance between L_{lk}, C_{MOS} and C_{TR} provides a sinusoidal voltage across the capacitance that reaches a maximum at one fourth of the resonant period, $\delta\tau_{max} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L_{lk}C}$, where $C = C_{MOS} + C_{TR}$. Similarly, the dead time required between Q1 and Q3 is determined using $4C_{MOS}V_{IN} + C_{TR}V_{IN} = I_P\delta_{\tau 1}$, where $4C_{MOS}V_{IN}$ corresponds to twice the charge stored in the nonlinear drain-source capacitance of the MOSFET. SPIC provides a feature by which the dead time between the turn ON and turn OFF of the switches in one leg of the bridge can be externally programmed. Figure 8 shows how control inputs A and B are used to program this dead time. The control inputs are the select inputs for the multiplexer and hence determine the number of stages by which the input PWM signal is delayed.

2.2. *Fault protection and soft start*

The fault-protection circuit for control (shown in Fig. 9) provides a shutdown under overcurrent sensing at the load and under-voltage conditions. The current-fault circuit imple-

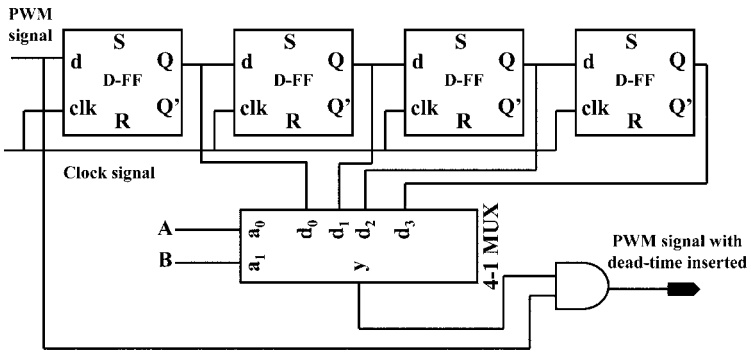
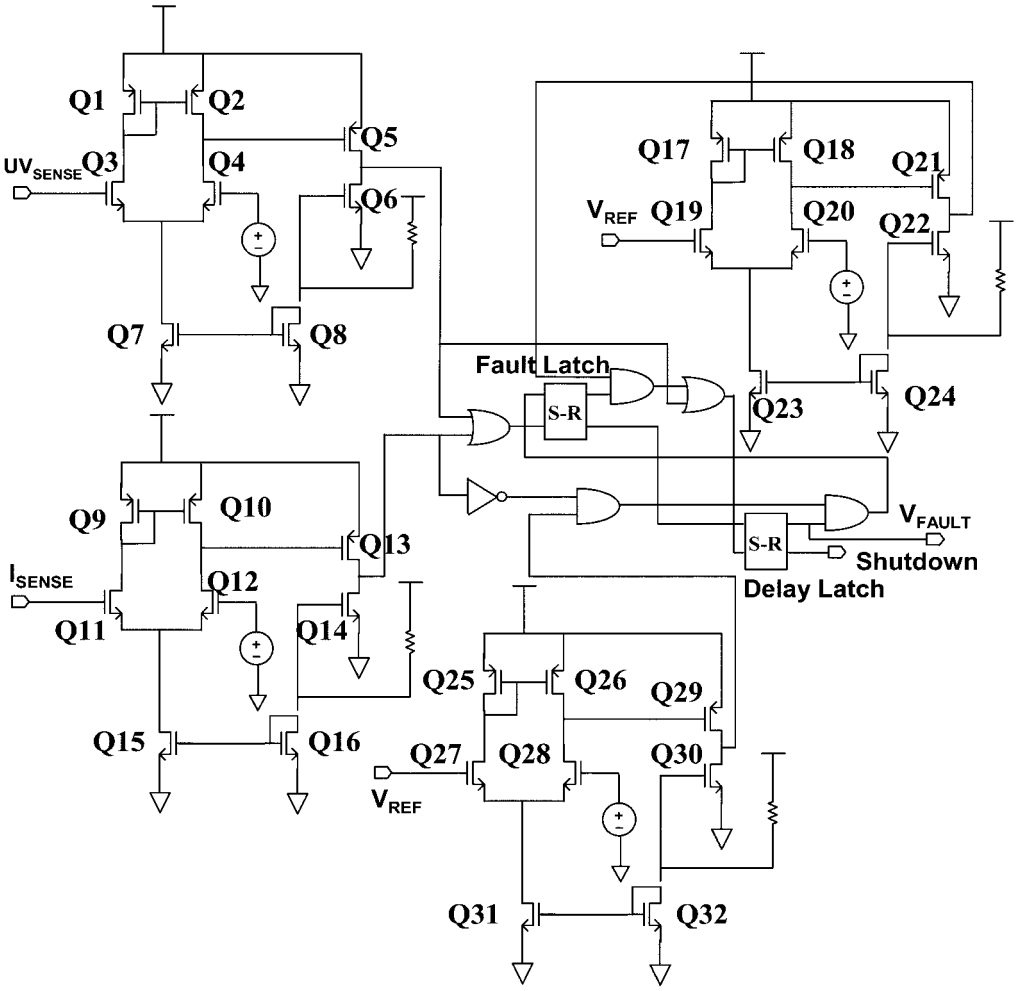


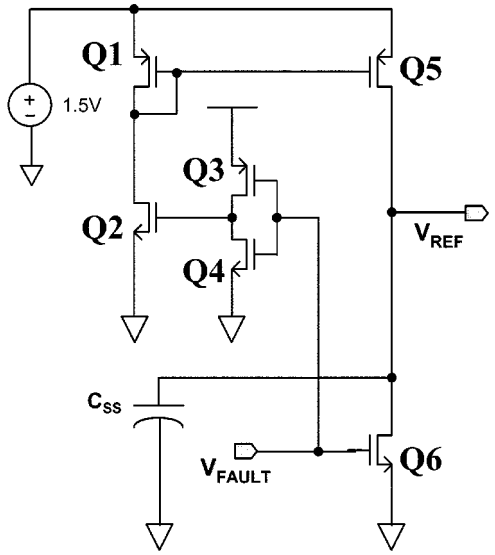
FIG. 8. Externally programmable dead-time circuitry for the FB controller.



$(W/L)_{Q1}$ = 150/1.6	$(W/L)_{Q9}$ = 150/1.6	$(W/L)_{Q17}$ = 150/1.6	$(W/L)_{Q25}$ = 150/1.6
$(W/L)_{Q2}$ = 150/1.6	$(W/L)_{Q10}$ = 150/1.6	$(W/L)_{Q18}$ = 150/1.6	$(W/L)_{Q26}$ = 150/1.6
$(W/L)_{Q3}$ = 150/1.6	$(W/L)_{Q11}$ = 150/1.6	$(W/L)_{Q19}$ = 150/1.6	$(W/L)_{Q27}$ = 150/1.6
$(W/L)_{Q4}$ = 150/1.6	$(W/L)_{Q12}$ = 150/1.6	$(W/L)_{Q20}$ = 50/1.6	$(W/L)_{Q28}$ = 150/1.6
$(W/L)_{Q5}$ = 300/1.6	$(W/L)_{Q13}$ = 300/1.6	$(W/L)_{Q21}$ = 300/1.6	$(W/L)_{Q29}$ = 300/1.6
$(W/L)_{Q6}$ = 300/1.6	$(W/L)_{Q14}$ = 300/1.6	$(W/L)_{Q22}$ = 300/1.6	$(W/L)_{Q30}$ = 300/1.6
$(W/L)_{Q7}$ = 100/1.6	$(W/L)_{Q15}$ = 100/1.6	$(W/L)_{Q23}$ = 100/1.6	$(W/L)_{Q31}$ =100/1.6
$(W/L)_{Q8}$ = 150/1.6	$(W/L)_{Q16}$ = 150/1.6	$(W/L)_{Q24}$ = 150/1.6	$(W/L)_{Q32}$ = 150/1.6

FIG. 9. Implementation of fault-protection scheme.

ments a full-cycle restart operation using a pair of S-R latches. When the current-sensing input (OC_{SENSE}) at the non-inverting input of the current comparator exceeds the internally set reference voltage of 2 V, the fault latch is set. This disables the gate drive signals, i.e. Shutdown is activated, which forces the output to the OFF state. A soft-start cycle is also



(W/L)Q1 = 3/1	(W/L)Q2 = 10/1	(W/L)Q3 = 20/1
(W/L)Q4 = 10/1	(W/L)Q5 = 20/1	(W/L)Q6 = 10/1

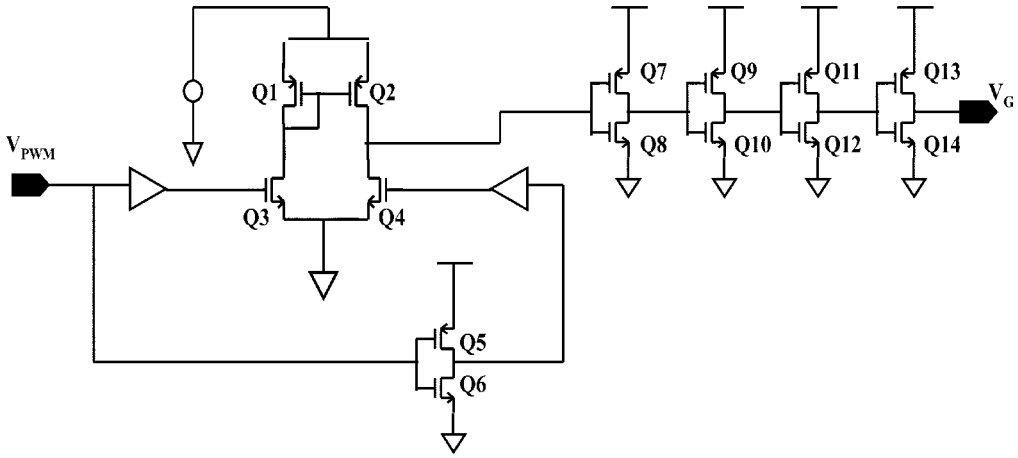
FIG. 10. Soft-start circuit.

initiated. Even if this input falls below 2 V, the fault latch does not reset until the soft-start capacitor voltage falls below an internally fixed voltage of 0.2 V. When these conditions are met and no other faults are detected, the fault latch is reset and normal system operation is resumed.

The soft-start mechanism controls the reference voltage at the input of the error amplifier. This provides a control in the start-up duty cycle for a monotonic increase in the output voltage without overstressing the power devices. The schematic for this implementation is shown in Fig. 10. During start-up (provided no other faults are detected, i.e., V_{FAULT} is low), the external capacitor C_{SS} charges exponentially through a current mirror to the steady-state reference voltage of 1.5 V. Two soft-start circuits are used in the design, one for the PFC and the other for the FBZVS converter.

2.3. *Design of gate drivers*

SPIC can directly fire the three low-side and two high-side power devices in the DPS. The low-side driver is implemented using a series of cascaded inverters, with each inverter stage being progressively larger to achieve lower driving impedance. Using a simple RC model of the inverter, a scaling factor of 3 is calculated for minimum delay through the stages. The power dissipation of the circuit includes static, dynamic and short-circuit power dissipation. Static power dissipation of CMOS inverters is mainly due to the substrate leakage current which is very small. The dynamic power dissipation is $P_d = f*c*V_{DD}^2$ where V_{dd} is the supply voltage, *f*, the switching frequency, and C, the load capacitance. Short-circuit power dissipation is due to the fact that two transistors will be conducting simultaneously, during switching, and hence will result in current flowing from V_{dd} to ground. Both dynamic



$(W/L)_{Q1}$ = 150/1.6	$(W/L)_{Q5}$ = 300/1.6	$(W/L)_{Q9}$ = 50/1.6	$(W/L)_{Q13}$ = 200/1.6
$(W/L)_{Q2}$ = 150/1.6	$(W/L)_{Q6}$ = 300/1.6	$(W/L)_{Q10}$ = 50/1.6	$(W/L)_{Q14}$ = 200/1.6
$(W/L)_{Q3}$ = 150/1.6	$(W/L)_{Q7}$ = 25/1.6	$(W/L)_{Q11}$ = 100/1.6	
$(W/L)_{Q4}$ = 150/1.6	$(W/L)_{Q8}$ = 25/1.6	$(W/L)_{Q12}$ = 100/1.6	

FIG. 11. Implementation of the low-side gate driver.

and short-circuit power dissipation increase with frequency. Hence, these buffer circuits need extra attention to minimize power dissipation. The ratio between two adjacent stages for minimum power dissipation is decided by V_{DD}, C, required signal rise and fall times, and other process parameters. Since the sensitivity of delay to changes in scaling factor is not particularly strong, a slightly larger scaling factor can be used instead of 3 to get the minimum power dissipation and less stages. Too many stages will also result in higher power dissipation. We used four stages to optimize these factors. The load capacitance is the gate-source capacitance of the power MOSFET and is about 1200–1300 pF. Figure 11 shows the schematic of the low-side gate-driver [13]. It comprises of a level-shifting stage, followed by a series of buffers. The level shifter translates the 0–5 V logic signal (V_{PWM}) to the required level of 0–12 V. This function is performed by a differential amplifier stage with a constant current sink. The output from this stage is then fed to a number of buffer stages to achieve the desired drive current to turn on the power switch. The number of stages in the buffer driver and their dimensions were optimized without degrading the total buffer propagation delay. Buffer sizing is calculated using $n = \ln(C_m/C_a)$, where n is the number of stages, C_m, the capacitive load driven by the buffer (gate capacitance of the power MOSFET) and C_a, the capacitance of a minimum-sized inverter. Here n is 4 and sizing factor is 2. A combination of bootstrap and charge-pump techniques is implemented to power the gate circuits, which drive the two high-side switches in the full-bridge converter module. The bootstrap mechanism sources the high instantaneous current needed for turning on the power device, while the charge-pump provides enough current to maintain bias voltage on the upper driver sections and power device. The schematic for the high-side driver is shown in Fig. 12 [13]. Besides the digital logic shown, all the other devices were implemented using standard-dimension high- voltage DMOS devices from Philips dis-

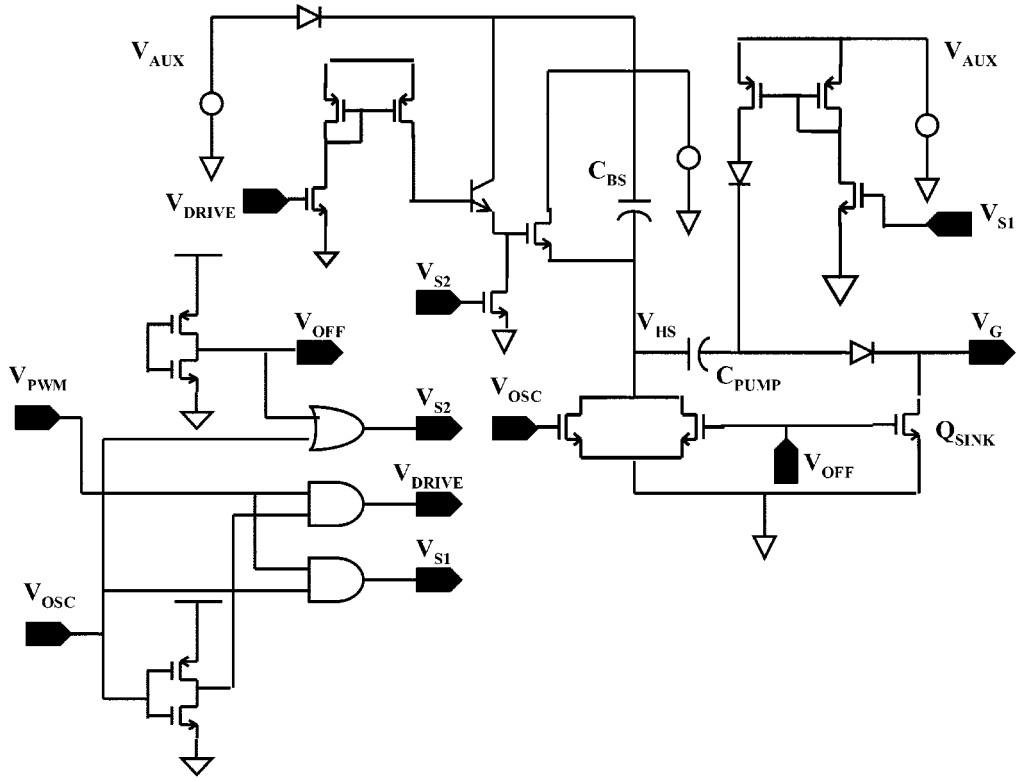


FIG. 12. Architecture of the charge-pump-based high-side gate driver.

cussed later in this section. The length of these devices is fixed at 2μ. The main drawback of bootstrapping techniques used alone is that it does not permit a 100% duty cycle. However, in this case, the bootstrap capacitor (C_{BS}) is periodically fed at a frequency which is ten times higher than the switching frequency of the DPS. The charging path for the bootstrap and charge-pump capacitor (C_{PUMP}) is provided by a switch which is driven by an internal square wave generator (V_{OSC}) that oscillates with a 50% duty ratio at 1 MHz. Switch S_1, which is connected to the high-side floating voltage (V_{HS}), is implemented using a DMOS. The operation of the driver can be classified in three phases.

In phase 1, the oscillator is on and hence the bootstrap capacitor CBS charges to its supply voltage (V_{AUX}). The charge-pump capacitor C_{PUMP} sinks in current from the current-mirror. In this interval, the PWM drive signal for the DMOS (V_{DRIVE}) is low. During phase 2, the oscillator turns off and the PWM signal is high. Through a current-mirror, the capacitor C_{BS} now sources current into the base of the *n-p-n* transistor. This transistor sources an amplified gate current to trigger S_1. Now the high-side floating voltage and the voltage across the charge-pump capacitor are in series with the gate of the power device. In phase 3, the PWM signal turns low and the sink transistor (Q_{SINK}) completely discharges the gate-source capacitance of the power device. The charge-pump capacitor discharges through this

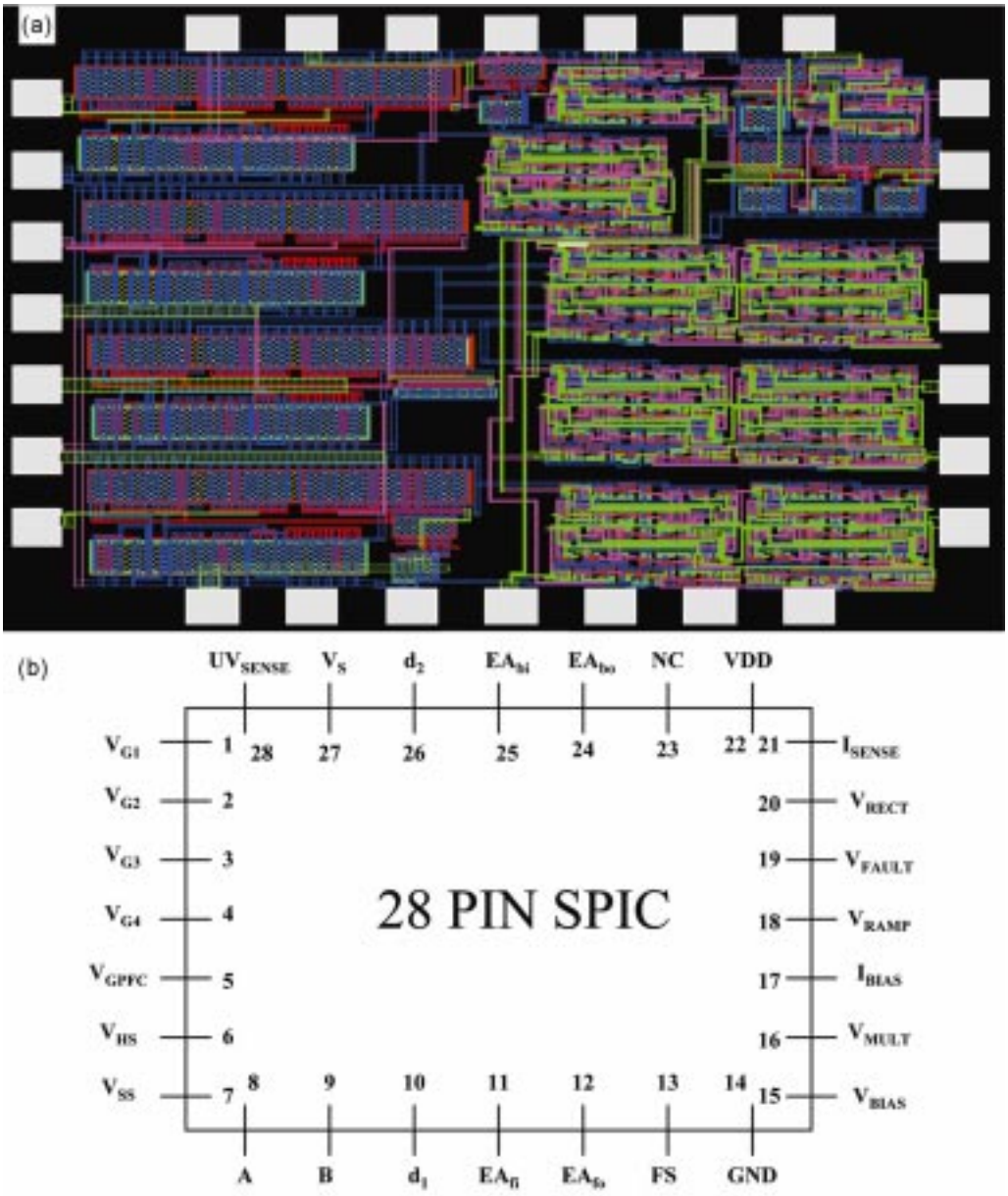


FIG. 13. (a) Layout of SPIC, and (b) the proposed pin out for the 28-pin SPIC.

transistor to its reset state. We used DMOS models from Philips Semiconductors to implement the high-voltage devices. The model files for the NMOS and PMOS high-voltage devices (*n*- and *p*-channel-enhancement DMOS) are as follows: the threshold voltage of these devices is +/– 0.5 V for the *n*- and *p*-channel devices, respectively. A number of such de-

Table II
Pinout description of SPIC

Isense	Sensed inductor current
Vrect	Line voltage template
Vfault	This pin indicates the occurrence of a fault due to short circuit or shoot-through.
Vramp	Output of the internal ramp oscillator
Ibias	This pin sets the bias current for the operational amplifier stages. It be connected to VDD through a 180 Ω resistor.
Vmult	Output of the analog multiplier.
Vbus*	This pin must be connected to the scaled down bus voltage being fed to SPIC.
$V_{G1\text{-}4}$	Gate drive signals for the four power devices in FB-ZVS.
V_{GPFC}	Gate drive signal for PFC.
V_{ss}	Soft-start pin. This pin is connected to an external capacitor and controls the rate of rise of the reference voltage fed to the error amplifier.
V_{HS}	This pin is connected to the high-side floating voltage node and is internally connected to the high-charge pump drivers.
A, B	These are input pins that can be used to externally program the dead-time period between the turn-off and turn on of two power devices in the same leg of the bridge.
d1	Duty ratio signal at the output of the inner current loop. This signal is being fed internally to PWM comparator for PFC.
EAfi	This pin is internally connected to the error amplifier for the PFC outer loop control.
EAfo	Output of the error amplifier for PFC.
FS	A capacitor from FS to GND selects the PWM oscillator frequency.
GND	Ground reference. All bypass and timing capacitors connected to GND must have short leads. All voltages are referenced to GND.
UV	Under-voltage sense pin.
Vs	This pin is connected to the feedback signal from the output of DPS.
d2	Duty ratio signal at the output of the voltage mode controller for FB-ZVS.
EAbi	This pin is internally connected to the error amplifier for FB-ZVS.
EAbo	Output of the error amplifier for FB-ZVS
VDD	Positive supply rail

vices can be effectively paralleled by changing the multiparameter, i.e. multiplication factor. The doping concentration of the substrate is set to a default value of 10^{15} cm^{-3}.

2.4. *SPIC layout*

Using the concepts outlined in Sections 2.1 and 2.3, we demonstrate a layout of SPIC in Cadence using a 0.25 μm TSMC-CMOS technology (Fig. 13(a)). The sizing of the devices for all the components and layouts of some key components have been described in Section 2. A 28-pin package is selected for the SPIC prototype (Fig. 13(b)). Apart from pins present in typical controller ICs for such applications, certain additional pins for debugging the controllers are included for the prototype device. These pins can be removed for commercial production and the package can be altered accordingly. The description of the functionality of each pin is given in Table II.

3. Results

The performance of the PFC-FBZVS converters, being simulated in Saber Designer, is tested along with SPIC, which is functionally simulated in Cadence. This native simulation

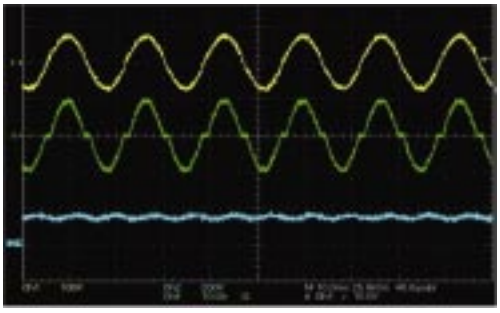


FIG. 14. Steady-state performance of the PFC shows that the line voltage (top trace) is in phase with the line current (middle trace), which establishes unity PF operation. The output bus voltage (bottom trace) of the PFC shows a small 120 Hz ripple.

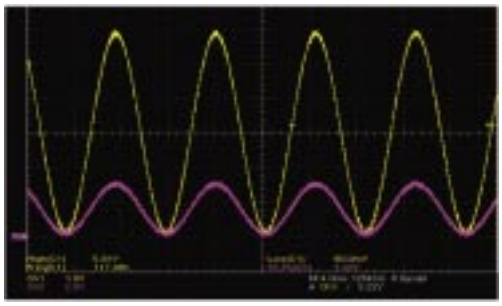


FIG. 15. Operation of the analog multiplier shows the input (yellow) and the output (pink) signals.

is accomplished using Cadence Frameway integration. The details of the simulation are outlined in Lokhandwala [13] and are not replicated here due to paucity of space.

Subsequent to the satisfactory simulated performance of the SPIC-controlled PFC-FBZVS converter, a discrete experimental validation of SPIC and PFC-FBZVS is conducted. The output power for the PFC-FBZVS converter is 250 W for an input rms voltage of 60 V. The switching frequencies of the PFC and the FBZVS converters are both 100 kHz. The experimental results for the front-end PFC converter are shown in Fig. 14. It shows that the current through the inductor (I_{PFC}) is in phase with the single-phase input voltage, illustrating a near unity power-factor operation. The output voltage of the PFC stage is the bus voltage (also shown in Fig. 14), which is fed to the FBZVS converter. It contains a 120 Hz second harmonic which is filtered by the low-bandwidth outer voltage loop of the PFC controller. The outer voltage-loop controller provides a fixed current reference for the inner current loop, which is then fed through an analog multiplier and multiplied with scaled rectified line voltage. The output of the multiplier is a reference signal for the inner current loop. Figure 15 shows an experimental result for the PFC current reference.

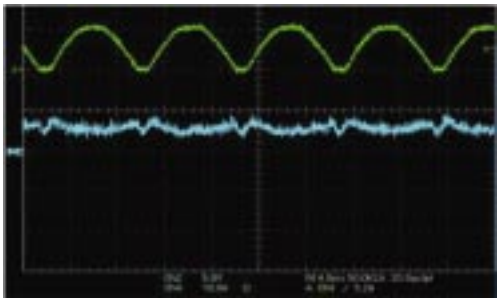


FIG. 16. The output of the PFC current-mode controller, which is proportional to the duty ratio, matches the characteristic of a PFC.

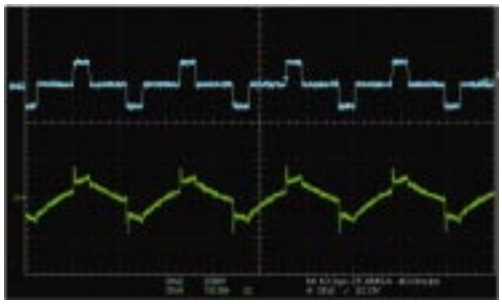


FIG. 17. Output voltage of the transformer secondary (top trace) and transformer primary current (bottom trace).

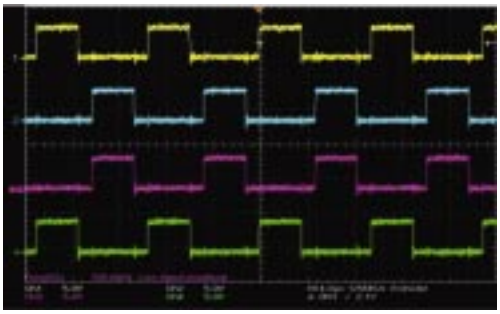


FIG. 18. Phase-shifted PWM signals for the four switches of the FBZVS converter.

The difference between the current reference and the inductor current of the PFC is fed to its current controller. The controller output, which is proportional to the duty ratio, is fed to the pulse-width modulator. Hence, we expect the duty ratio to reach its maximum at the zero crossing of the input voltage (or inductor current under unity PF operation) and minimum when the input voltage or inductor current reaches its peak. The operation of the current-mode controller is verified through experimental result shown in Fig. 16.

Figure 17 shows the output of the FBZVS converter. It shows the behavior of the voltage and current at the secondary and primary of the isolation transformer. The experimental results match the simulation results [13] as well as previously published results on FBZVS [9]. The phase-shifted PWM signals for the four switches of the FBZVS, as shown in Fig. 18, further validate the results.

Next, in Figs 19 and 20, we show the performance of the high-side gate driver (under varied load conditions), which is operated using a combination of bootstrap and charge-pump techniques to drive the two high-side switches of the FBZVS stage. The bootstrap mechanism sources the high instantaneous current while the charge-pump provides enough bias voltage on the upper driver sections and power device. The bootstrap capacitor is peri-

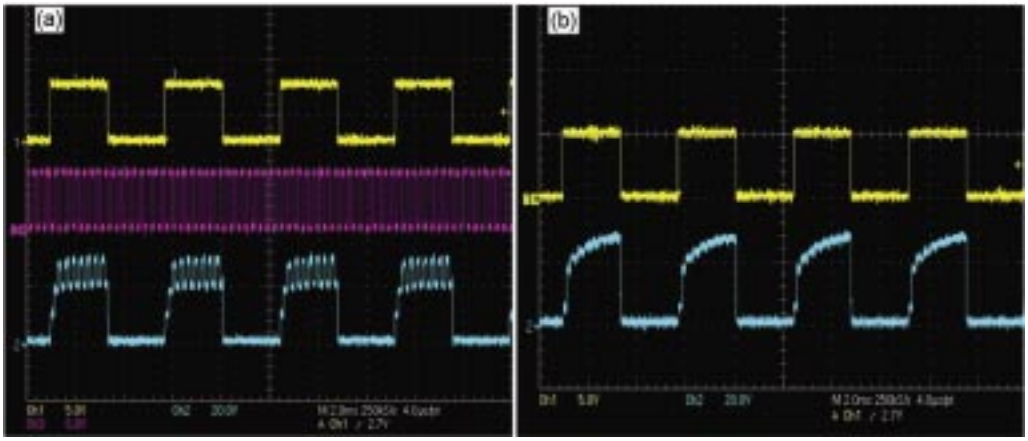


FIG. 19. High-side gate driver results (a) control signal (top), oscillator output (middle), and driver output (bottom) without any load, and (b) control signal (top) and driver output (bottom) when connected to a power MOSFET.

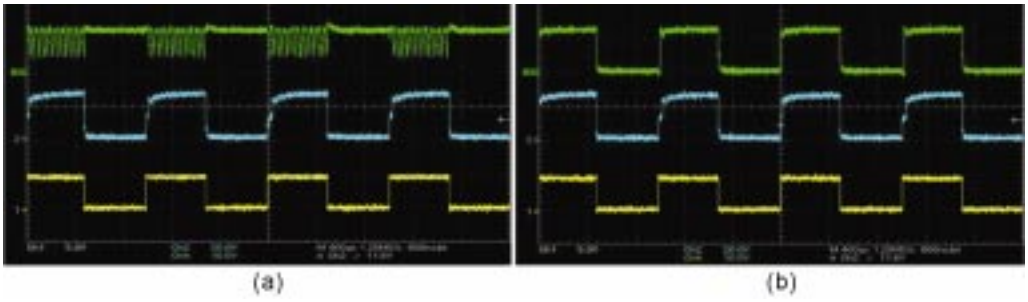


FIG. 20. (a) Control signal (bottom), driver output (middle) and bootstrap capacitor voltage (green); and (b) control signal (bottom) driver output (middle) and voltage across the charge-pump capacitor.

odically fed at a frequency, which is ten times higher than the switching frequency of the power device. The high-frequency oscillator refreshes the bootstrap capacitor continuously. This capacitor switches the high-voltage DMOS which is connected to the bus voltage.

The voltage across the bootstrap and charge pump capacitors is shown in Fig. 21. We can observe that the bootstrap capacitor discharges when the PWM signal and oscillator are high. During the remaining part of the switching cycle it remains charged at 12 V. Similarly, the charge-pump capacitor stays charged at 12 V when the PWM signal is high.

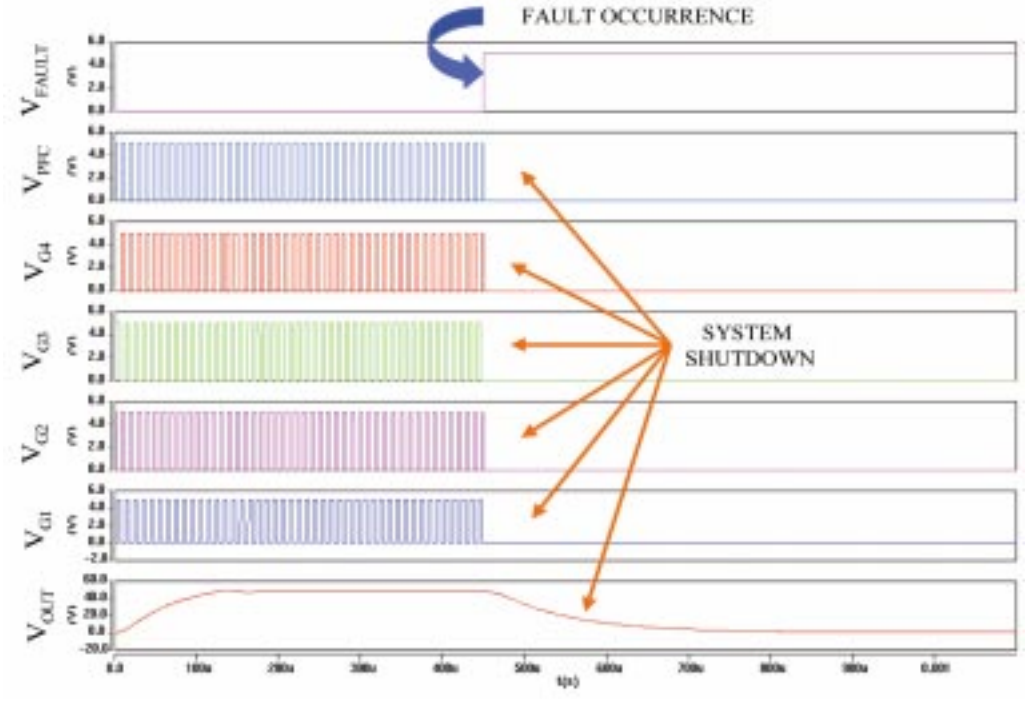


FIG. 21. Fault-detection response of the DPS.

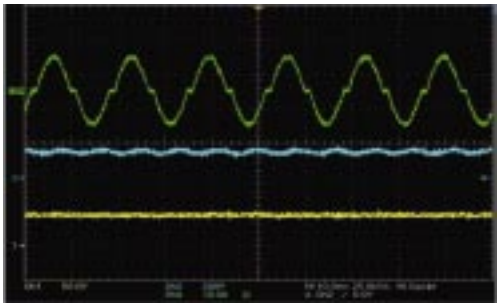


FIG. 22. Steady-state performance of the DPS: (top to bottom traces) input current of the PFC converter, input (bus) voltage of the FBZVS converter, and the output voltage of the DPS.

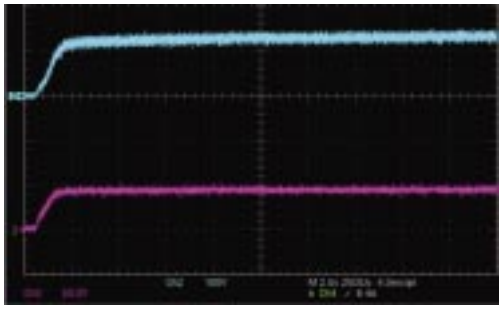


FIG. 23. Start-up response of the DPS: top trace; bus voltage and bottom trace; output voltage.

Next, we tested the DPS for its response under fault condition. This fault could be either at the load (load-short circuit) or an under-voltage condition. The behavior of the DPS during a fault occurrence is shown in Fig. 21. V_{PFC} is the gate signal for PFC, while $V_{GS1\text{-}4}$ are the PWM gate signals for the four power devices in the full-bridge converter. V_{OUT} is the output voltage of the DPS regulated at 48 V. When a fault occurs (V_{FAULT} = 1), the system shuts down. Hence, the five power devices are protected by inactivating their gate-drive signals and the output voltage of the power system decays to zero.

Finally, in Figs 22–24, we illustrate the steady-state performance of the overall PFC-FBZVS DPS, start-up and transient responses of the DPS. All the responses are satisfactory.

5. Summary and conclusion

We present the design and discrete validation of a smart power integrated circuit (SPIC) for a distributed power system (DPS) comprising a single-switch ac/dc power-factor correction (PFC) front-end converter cascaded to a dc/dc full-bridge zero-voltage switching (FBZVS) converter. The block-level architecture of the SPIC is explained in depth along with other

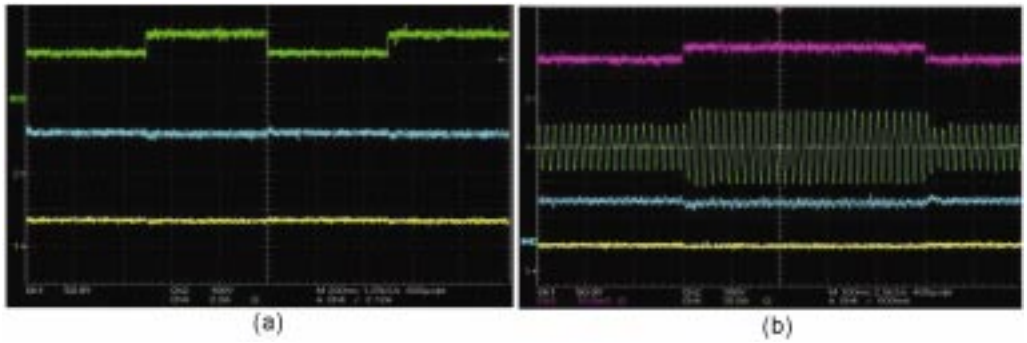


FIG. 24. Load transient response of the DPS: (a) load current (top), bus voltage (middle), and output voltage (bottom), and (b) load current (top), source current (second from top), PFC output voltage (third from top), and DPS output voltage (bottom).

mixed-signal components used in the design. Finally, several key experimental results of the DPS controlled by the discrete SPIC are demonstrated. The performances of this controller are gauged under steady-state as well as transient conditions and are found to be excellent.

The proposed SPIC leads to higher power density, reduced design cycle time, and an enhanced reliability of the DPS due to integration of gate-drivers and controls and its key features are as follows:

(i) Integrates current- and voltage-mode controllers for the PFC and the FBZVS converters, respectively, and a more reliable two-stage fault protection scheme on the same IC;
(ii) Directly fires the two high-side and three low-side power devices of the DPS;
(iii) Combination of bootstrap and charge-pump techniques is used; as such, the maximum duty ratio is 100% and the turn-on times of the high-side devices are independent of the low-side devices; only one external power supply is needed;
(v) Incorporates protection features such as under-voltage lockout, over-current protection, adaptive shoot-through protection, and soft-start capability.

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