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A PWM scheme for a 3-level inverter cascading two 2-level inverters

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Abstract

This paper shows that 3-level inversion can be achieved by connecting two 2-level inverters in cascade. Two isolated power supplies with DC link voltages are required for the proposed circuit topology. The voltages constitute half of that of a conventional 3-level inverter topology. Neutral point fluctuation is absent in the proposed scheme when compared to conventional neutral point clamped 3-level inverter. A sine-triangle-based PWM scheme is presented for the proposed topology.

Keywords: Multilevel inverter, PWM technique.

1. Introduction

Three-level inverters have attracted the attention of researchers since their introduction by Nabae *et al.* [1] in 1981. Though simple and elegant, neutral-clamped circuit topology has a few disadvantages. Neutral point fluctuation is commonly encountered as the capacitors connected to DC-bus carry load currents. Also, there is ambiguity regarding the voltage rating of the semiconductor devices, which are connected to the neutral point. This calls for a conservative selection of devices for reliable operation, which, however, increases cost.

Various alternative circuit topologies have been suggested in the literature. H-bridge topology [2], [3] eliminates the problem of neutral fluctuation, but requires three isolated power supplies. Suh and Hyun [4] have suggested an improvization of the conventional neutral clamped inverter in which a capacitor is connected across the neutral clamping diodes to ensure dynamic balancing of the voltage across the DC bus capacitors. This method alleviates the problem but does not eliminate it.

Three-level inversion may also be achieved with two 2-level inverters, driving an open-end winding induction motor from either end [5], [6]. The inverters in this case require isolated power supplies to eliminate the harmonic currents of the triplen order in the individual motor phases. Recently, Somasekhar *et al.* [7] have suggested an open-end winding induction motordrive, which obviates transformer isolation. But the DC bus utilization is slightly lower in this scheme when compared to the schemes proposed by Stemmler and Guggenbach [5] and Shivkumar *et al.* [6]

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In this paper, we suggest a new circuit configuration for a 3-level inverter which is realized by connecting two 2-level inverters in cascade. The DC link capacitors in this circuit do not carry the load currents and hence the voltage fluctuations in the neutral point are absent. Also, the circuit configuration needs two isolated power supplies compared to H-bridge topology, which requires three isolated power supplies to achieve 3-level inversion. However, the power semiconductor switches in one bank (three in number) in one of the inverters of this circuit have to be rated for the full DC link voltage.

2. Proposed 3-level inverter configuration

In the proposed 3-level inverter topology circuit, the cascade connection of two 2-level inverters accomplishes 3-level inversion (Fig.1a). The output phases of Inverter1 are connected to the DC input points of the corresponding phases in Inverter2.

Each inverter is powered with an isolated DC power supply, with a voltage of $V_{dc}/2$ (Fig. 1a). The symbols v_{A10}, v_{B10} and v_{C10} denote, respectively, the output voltages of the individual phases– A_1, B_1 and C_1 of Inverter1, with respect to point 'O'. Similarly, the symbols v_{A20}, v_{B20} and v_{C20} denote, respectively, the pole voltages of Inverter2.

The pole voltage of any phase of Inverter2 attains a voltage of $V_{dc}/2$ when i) the top switch of that leg in Inverter2 is turned on, and ii) the bottom switch of the corresponding leg in Inverter1 is turned on. Similarly, the pole voltage of any phase in Inverter2 attains a voltage of V_{dc} when i) the top switch of that leg in Inverter2 is turned on, and ii) the top switch of the corresponding leg in Inverter1 is turned on.

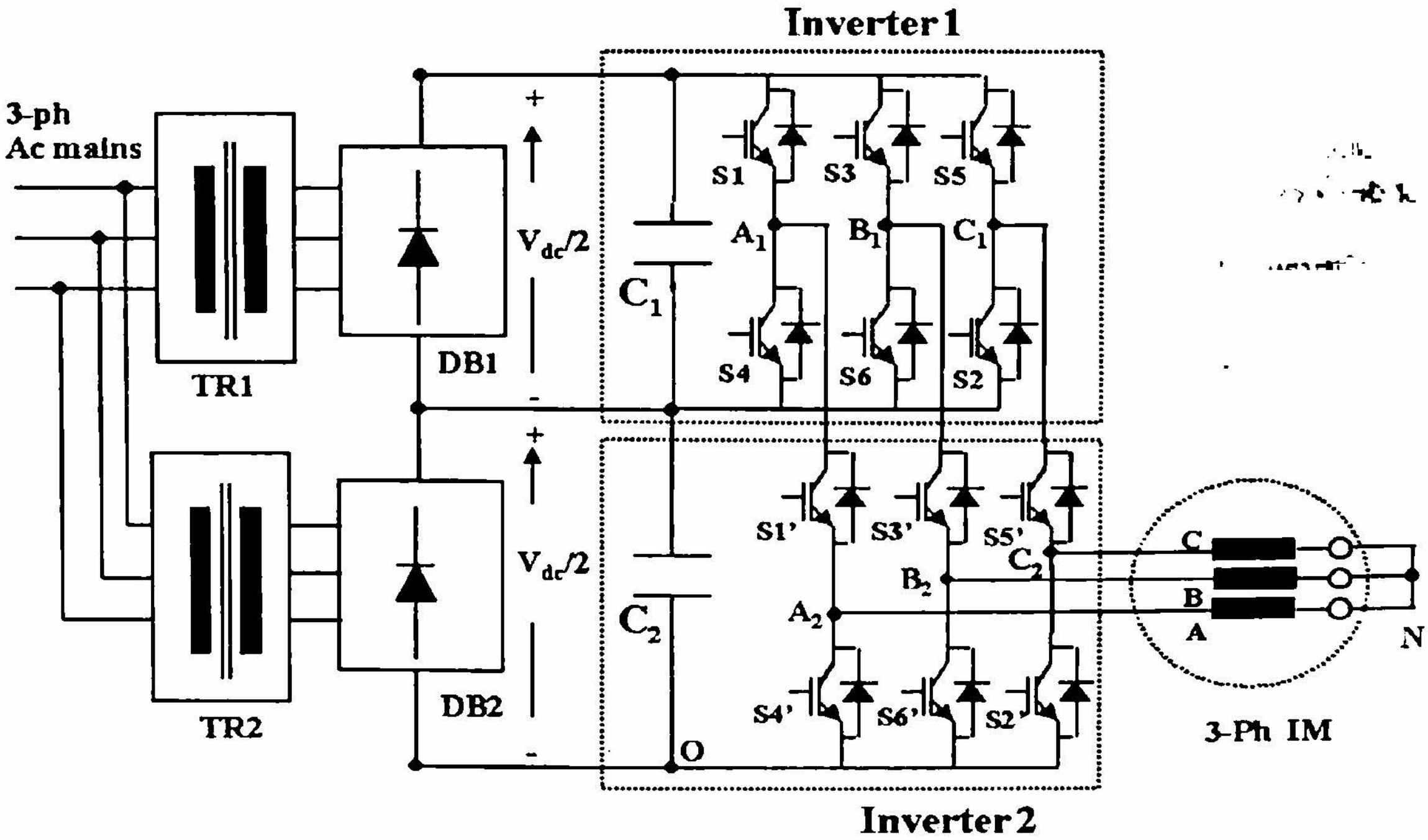

Fig.1a. The power circuit configuration of the proposed 3-level inverter.

Thus, the DC input points of individual phases of Inverter2 may be connected to a DC link voltage of either V_{dc} or $V_{dc}/2$ by turning on the top or the bottom switch of the corresponding phase leg in Inverter1.

Additionally, the pole voltage of a given phase in Inverter2 attains a voltage of zero, if the bottom switch of the corresponding leg in Inverter2 is turned on. In this case, the DC input point of that phase for Inverter2 is floating as the top and bottom switches are switched complementarily in any leg in a 2-level inverter. Thus, the pole voltage of a given phase for Inverter2 is capable of assuming one of the three possible values, 0, $V_{dc}/2$ and V_{dc}, which is the characteristic of a three-level inverter.

One of the advantages of the proposed circuit is that it can be operated as a conventional 2-level inverter in the lower output voltage range. This is accomplished by turning on the semiconductor devices in the lower bank of Inverter1, i.e. the devices S_4, S_6 and S_2 (Fig.1a) and only the devices of Inverter2 (S_1' through S_6') are switched following a suitable modulation scheme. Consequently, in this operating range, the switching losses are due entirely to the switching of one of these inverters and are expected to be lower than the conventional inverter topology. In the higher voltage range, both the inverters are switched based on modulation strategy. Another advantage of the proposed circuit configuration compared to H-bridge topology is that the former requires two isolated DC power supplies of $V_{dc}/2$ each, while the latter requires three.

However, the bottom bank switches of Inverter2 are to be rated for the full DC bus voltage of V_{dc} in the proposed scheme. For example, when the switches S1 and S1' are turned on in the A-phase legs of both the inverters, $v_{A20} = V_{dc}$. Consequently, switch S4' must be rated for V_{dc}. The switches in the top bank of Inverter2 need not be rated for the full DC link voltage of V_{dc} because the top switch of any phase leg of Inverter2 blocks the DC input voltage to Inverter2, when the corresponding bottom switch is turned on. Under these conditions, the bottom switches of the corresponding phases of Inverter1 may be turned on so that the top switches of the corresponding phases in Inverter2 need to block only a voltage of $V_{dc}/2$.

Triplen harmonic currents are absent in this case as the neutral point 'N' of the motor is not connected to point 'O'. Hence, all the triplen harmonic voltages appear across the points 'O' and 'N' (Fig. 1a). Table I depicts individual inverter states and the semiconductor switches turned on to realize that state. In Table I, a '+' and a '–' indicate, respectively, that the top and bottom switches in an inverter leg are turned on.

An example is presented in the following paragraph to determine the resultant space vector location for a space vector combination of 6-4' of the two inverters. From Table I, it may be noted that the combination 6-4' implies that the switching state for Inverter1 is (+ – +) and that for Inverter2 is (– + +).

The space vector $\mathbf{v_s}$ constituted by the pole voltages v_{A20}, v_{B20} and v_{C20} is defined as:

$$\mathbf{v_s} = v_{A2O} + v_{B2O}.e^{j(2\pi/3)} + v_{C2O}.e^{j(4\pi/3)}. \quad (1)$$

If Inverter1 assumes a state of '6' (+ – +) and Inverter2 '4' (– + +), it follows from the earlier discussion that

Table I
Inverter states for individual inverters

State of Inverter1	Switches turned on	State of Inverter2	Switches turned on
1 (+ − −)	S6, S1, S2	1' (+ − −)	S6', S1', S2'
2 (+ + −)	S1, S2, S3	2' (+ + −)	S1', S2', S3'
3 (− + −)	S2, S3, S4	3' (− + −)	S2', S3', S4'
4 (− + +)	S3. S4. S5	4' (− + +)	S3', S4', S5'
5 (− − +)	S4. S5, S6	5' (− − +)	S4', S5', S6'
6 (+ − +)	S5, S6, S1	6' (+ − +)	S5', S6', S1'
7 (+ + +)	S1, S3, S5	7' (+ + +)	S1', S3', S5'
8 (− − −)	S2, S4, S6	8' (− − −)	S2', S4', S6'

$$v_{A20} = 0 \; ; \; v_{B20} = V_{dc}/2 \; ; \; v_{C20} = V_{dc} \, . \tag{2}$$

Consequently, the space vector location for the above set of pole voltages is given by

$$\mathbf{v_s} = (0) + (V_{dc}/2).e^{j(2\pi/3)} + (V_{dc})e^{j(4\pi/3)} \, . \tag{3}$$

It may be verified that the tip of the space vector corresponding to the above pole voltages is located at point 'N' in Fig.1b. The space vector locations corresponding to the rest of the 63 combinations may similarly be determined. Figure 1b depicts that these space vector combinations are distributed over 19 space vector locations similar to a conventional 3-level inverter. All the space vector combinations and the space vector locations are shown in Fig.1b. Typical pole and phase voltage waveforms that are obtained experimentally are shown in Fig. 1c–f.

A DC link voltage of 300 V is used for experimentation ($V_{dc} = 300$ V). This means that individual inverters are operated with a DC link voltage of 150 V. The motor is run in open loop using the V/f control scheme. To demonstrate the working principle of this inverter scheme, space vector modulation has been employed, which was implemented using look-up table approach. The space vector combinations at each space vector location have been chosen in such a way that both the inverters are switched with only one transition during the subinterval period.

The top trace of Fig. 1c presents the experimentally obtained waveform of the output of phase-A of Inverter1 (v_{A1O}) in the mode of 2-level inversion. It may be recalled that Inverter1 is clamped in this operating mode as all of the switching devices in the bottom bank of Inverter1 (S2, S4 and S6) are turned on throughout the cycle of operation (clamped to state 8, Table I). Consequently, all the DC input points of Inverter2 attain a voltage of $V_{dc}/2$ as explained in Section 2. The bottom trace of Fig. 1c depicts the waveform of pole voltage of Inverter2 (v_{A2O}) in the mode of 2-level inversion and shows only two levels, 0 and $V_{dc}/2$. The triplen harmonic content in the pole voltage v_{A2O} is dropped across the points 'O' and 'N' (Fig. 1a) as explained earlier. Consequently, the individual motor phase voltages do not possess the harmonic components of the triplen order. Figure 1d presents the waveform of the motor phase voltage v_{A2N} in the mode of 2-level inversion.

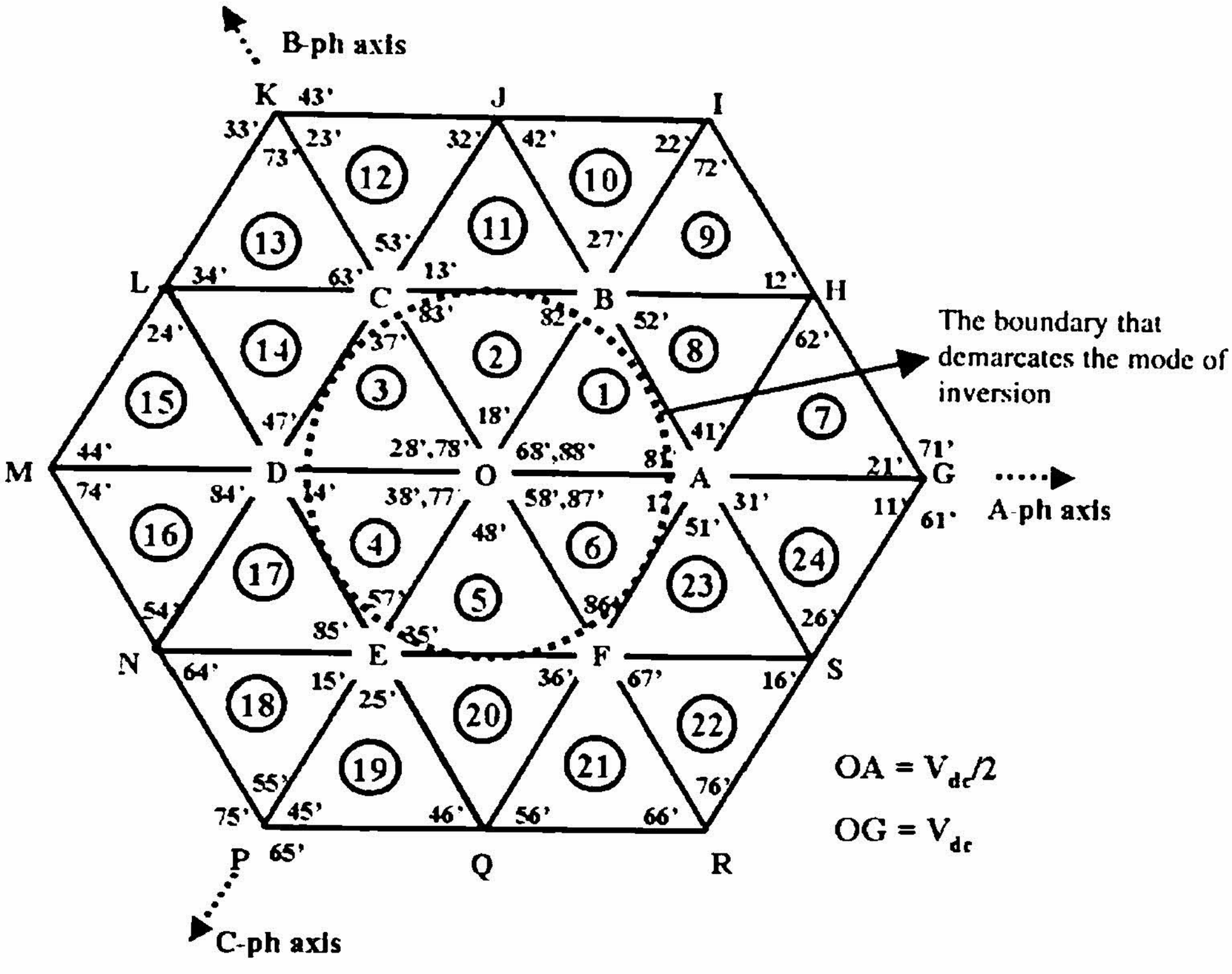

Fig.1b. The space-vector locations and combinations in the proposed circuit topology.

The top trace of Fig.1e presents the experimental waveform of the output of phase-A of Inverter1 (v_{A1O}), in the mode of 3-level inversion. As mentioned earlier, both the inverters are switched on in this operating mode. Consequently, the pole voltage waveform of Inverter2 (presented in the bottom trace of Fig.1e) shows all the three levels, 0, $V_{dc}/2$ and V_{dc}, which demonstrates the working principle of the proposed topology. Figure 1f depicts the experimentally obtained waveform of the phase voltage v_{A2N} in the mode of 3-level inversion. The phase voltage waveform in the 3-level mode of operation shows a 16-stepped profile compared to the six-stepped profile in the mode of 2-level inversion.

In this paper, a sine-triangle PWM scheme is also proposed for the inverter scheme. The scheme does not require look-up tables to realize the switching sequences as in the case of space vector modulation. Also, the switching criterion that there should be only one switching of the power devices of the constituent inverters during the subinterval of the sampling time period is automatically ensured in the sine-triangle PWM scheme [3].

3. A modified SPWM strategy for the proposed 3-level inverter

While two level-shifted triangular carrier waves are generally employed to compare the modulating sine wave to generate PWM signals for a 3-level Inverter [2], one bipolar triangular carrier wave is sufficient for a 2-level inverter.

As mentioned earlier, one of the important advantages of the proposed 3-level inverter is that it can be operated as a 2-level inverter in the lower output voltage range. This is accomplished by

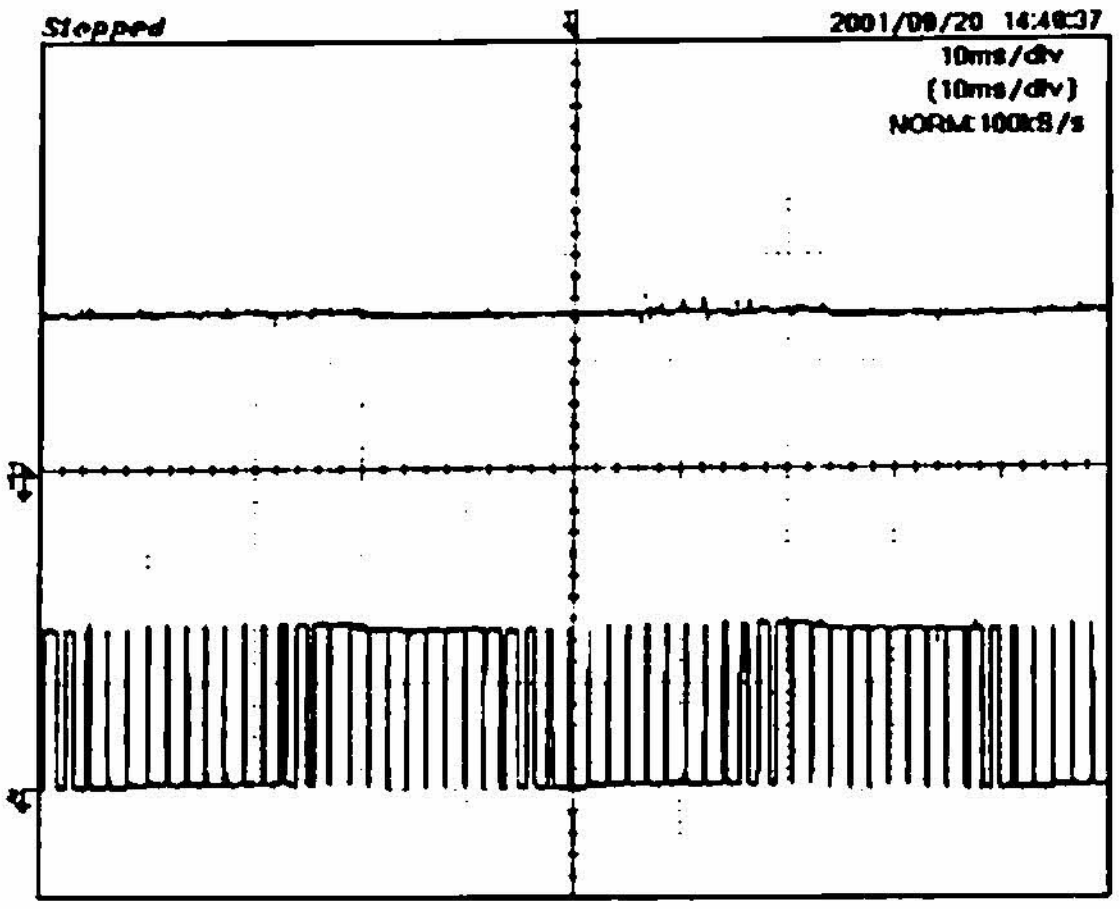

Fig. 1c. Experimental waveforms of the voltage v_{A1O} (top) and the pole voltage v_{A2O} (bottom) in the mode of 2-level inversion. Scale: X-axis: 10 ms/div and Y-axis: 100 V/div.

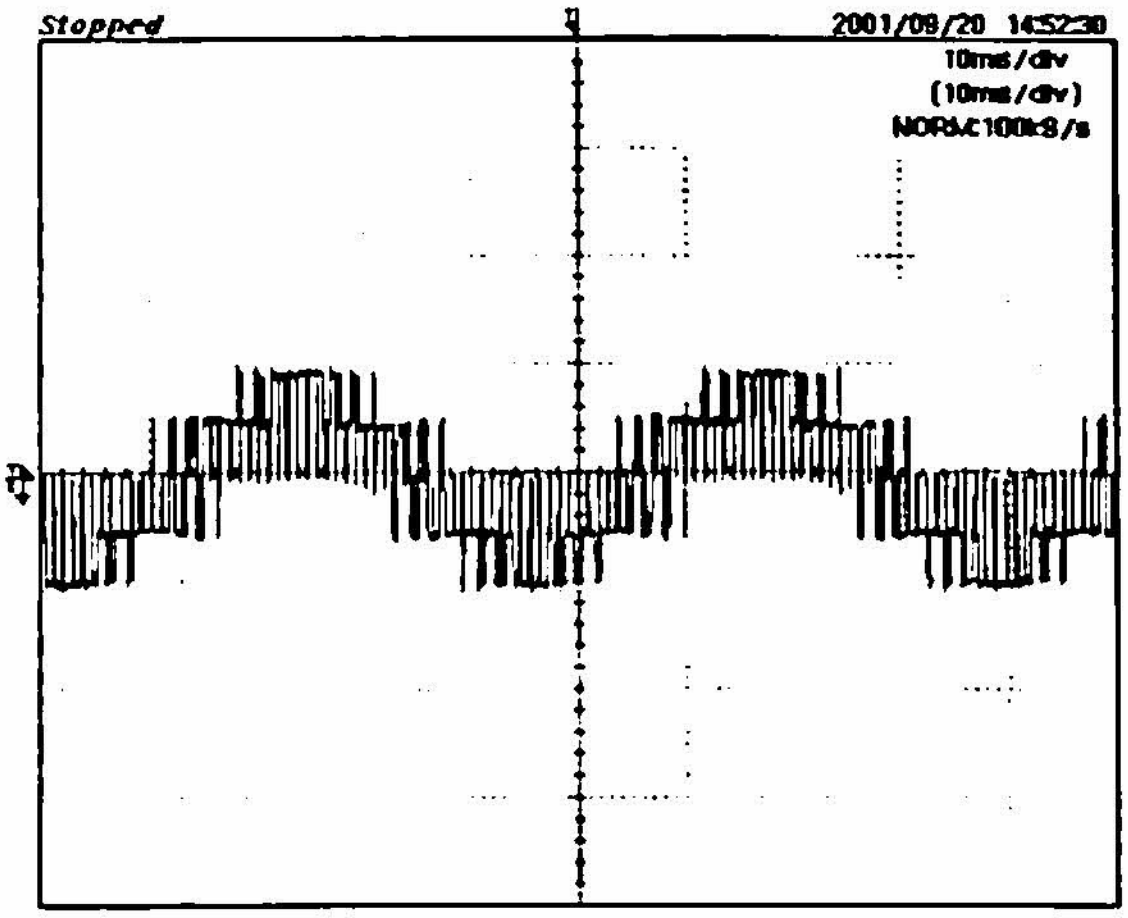

Fig. 1d. Experimental waveform of the phase-voltage v_{A2N} in the mode of 2-level inversion. Scale: X-axis: 10 ms/div and Y-axis: 100 V/div.

comparing the modulating sine wave with only one triangular carrier wave for the generation of PWM signals in the lower output voltage range and with two triangular carrier waves in the higher output voltage range.

Figure 2 illustrates the proposed SPWM strategy. To get a clear picture to facilitate the explanation of the proposed SPWM strategy, the frequency of the triangular carrier wave was chosen to be only 11 times that of the frequency of the modulating sine wave. Also, to simplify the illustration of the concept of the proposed SPWM strategy, it is assumed that the frequency of the modulating sine wave is constant. But, in reality, it is varied by the speed controller as in V/f control or the vector control. Also, the frequency of the triangular carrier wave will be significantly higher in practice.

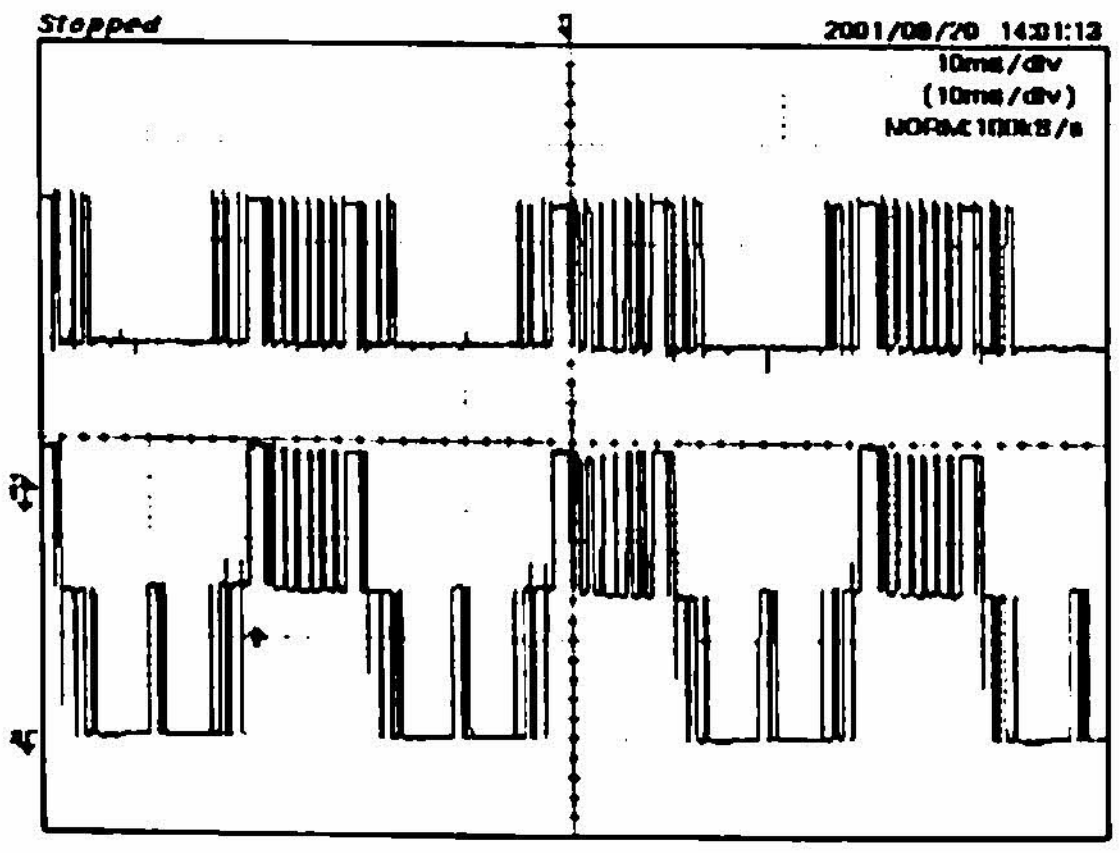

Fig. 1e. Experimental waveforms of the voltage v_{A1O} (top) and the pole voltage v_{A2O} (bottom) in 3-level inversion mode. Scale: X-axis: 10 ms/div and Y-axis: 100 V/div.

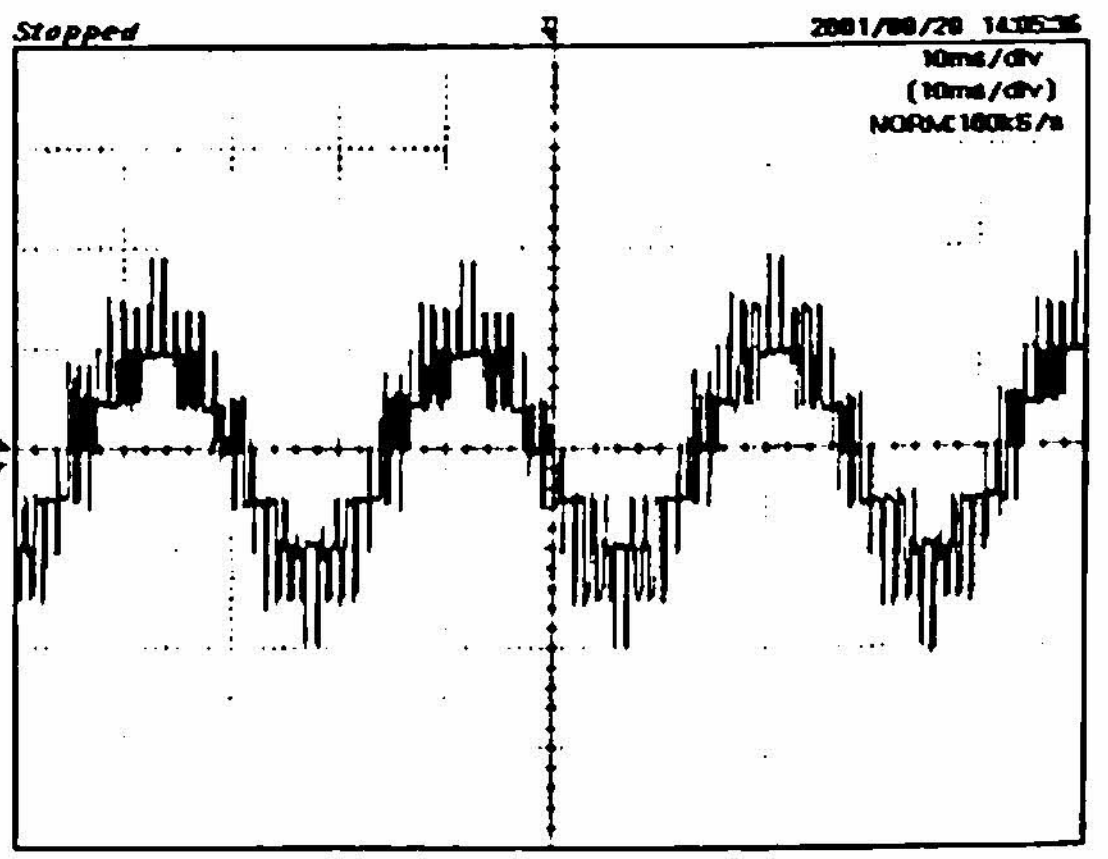

Fig. 1f. Experimental waveform of the phase-voltage v_{A2N} in 3-level inversion mode. Scale: X-axis: 10 ms/div and Y-axis: 100 V/div.

In the lower output voltage range, the modulating sine wave is compared with the lower bipolar triangular carrier wave centered on O_2 (Fig. 2a). A higher output voltage is obtained by increasing the modulation index, while operating in 2-level inversion mode (Fig. 2b). When the peak value of the modulating sine wave becomes exactly equal to the peak value of the lower triangular carrier wave as shown in Fig. 2b, it is given a bias equal to the peak value of the lower triangular carrier wave as shown in Fig. 2c. From now on, it is compared with both the upper and lower triangular carrier waveforms centered on O_3 (Fig. 2c), thus commencing the 3-level inversion mode. The output voltage can further be enhanced by increasing the peak value of the modulating sine wave, which is now centered on O_3 (Fig. 2d).

The harmonic spectrum of the motor phase voltage v_{A2N} operating in 2-level inversion mode which is on the verge of changing over to 3-level inversion (i.e. corresponding to the condition depicted in Fig. 2b) is presented in Fig. 2e. Figure 2f presents the harmonic spectrum of the phase voltage v_{A2N} operating in 3-level inversion mode, having just changed over from 2-level inversion mode (corresponding to the condition illustrated in Fig. 2c). The process of changeover is smooth as there is no change in the value of the fundamental component of the motor phase voltage v_{A2N} during the process of changeover. Figure 2g illustrates the simulated waveform of the motor phase voltage in 2-level operation mode (corresponding to the operating condition depicted in Fig. 2a). Figure 2h illustrates the simulated waveform of the motor phase voltage in 2-level operation mode, which is on the verge of changing over to 3-level operation (corresponding to the condition illustrated in Fig. 2b). Similarly, Fig. 2i depicts the simulated waveform of the motor phase voltage in 3-level operation mode, which is on the verge of changing over to 2-level operation (corresponding to the condition illustrated in Fig. 2c). From Figs 2h and i, it is evident that the motor phase voltage has a six-stepped envelope at changeover in both the modes of operation. Figure 2j presents the simulated waveform of the motor phase voltage in 3-level operation mode. It may be noted that the motor phase voltage has a six-stepped profile while operating in 2-level inversion mode and a 16-stepped profile while operating in 3-level inversion mode. Hence, one may expect a better spectral performance with 3-level compared to 2-level operation.

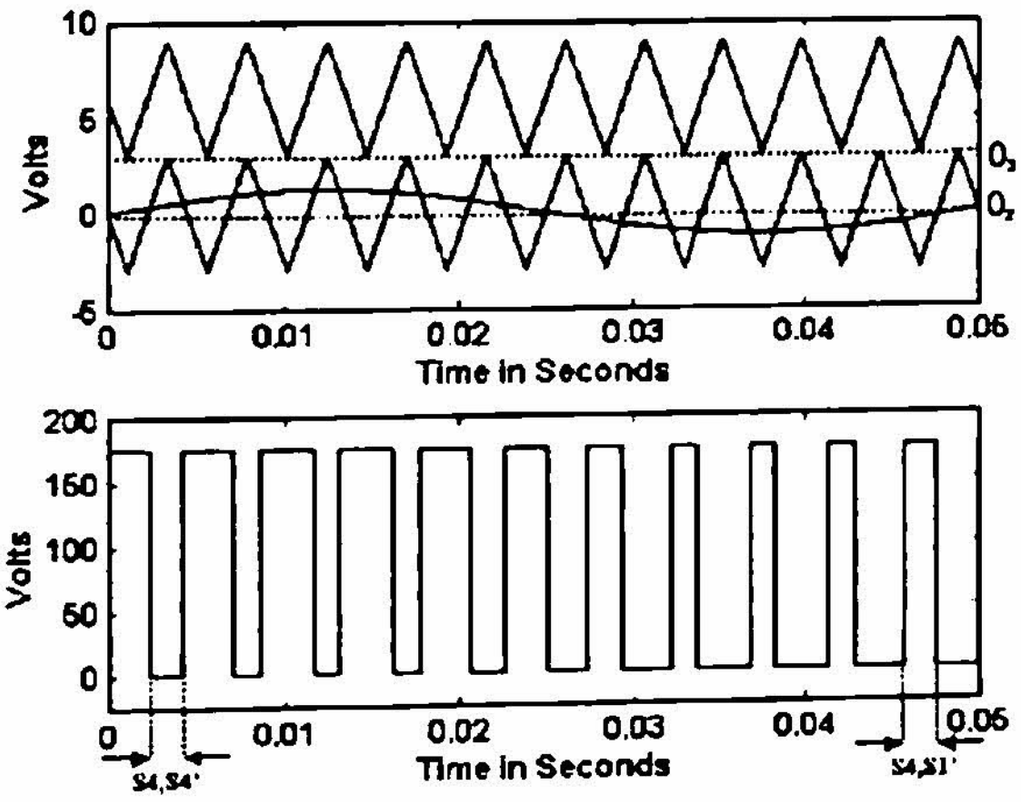

Fig. 2a. Operation of the proposed circuit in 2-level inversion mode.

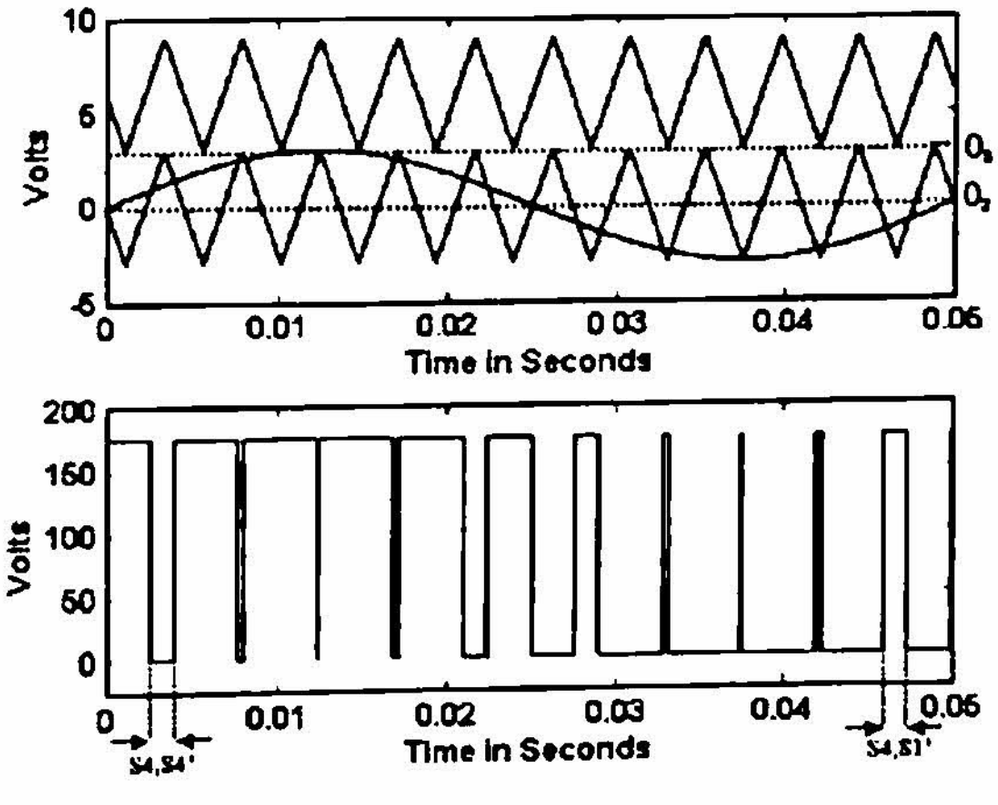

Fig. 2b. Operation of the proposed circuit in 2-level inversion mode on the verge of changeover to 3-level inversion mode.

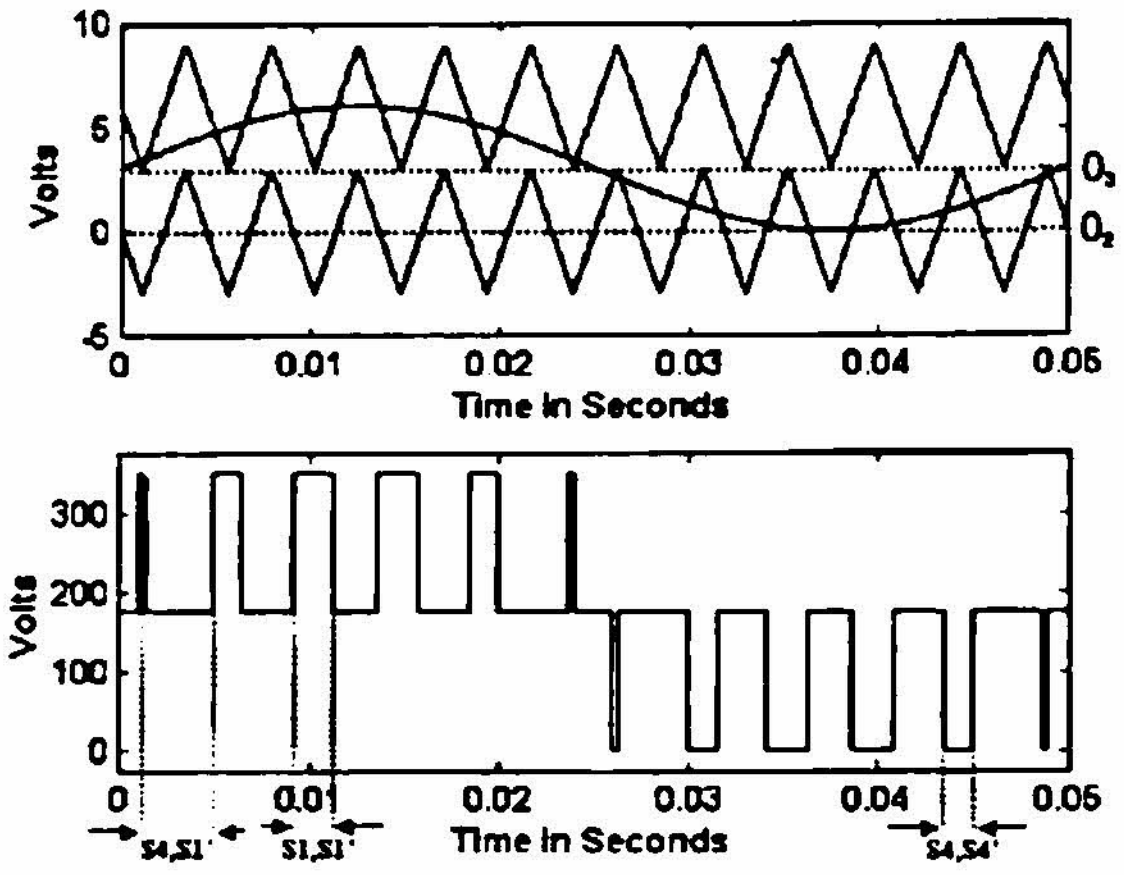

Fig. 2c. Commencement of the 3-level mode of operation of the proposed inverter circuit.

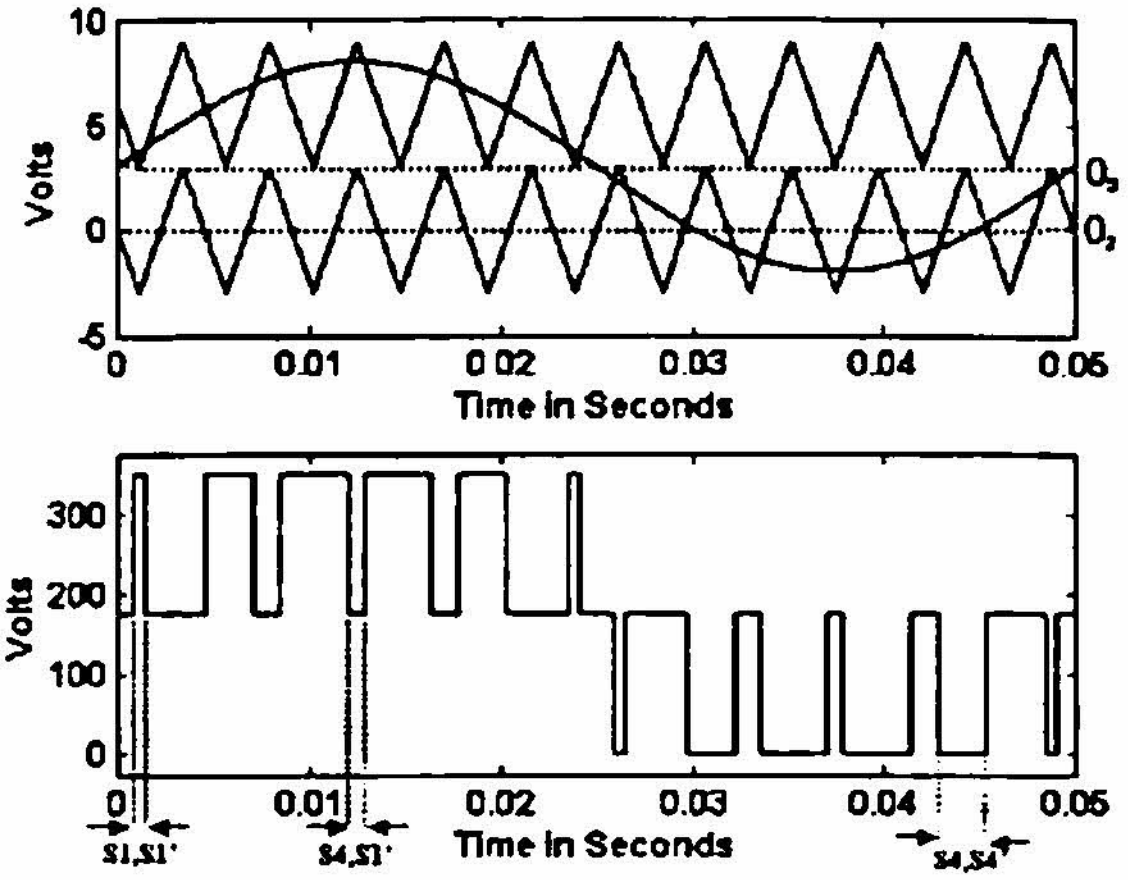

Fig. 2d. Operation of the proposed circuit in 3-level inversion mode.

4. Implementation of the proposed PWM strategy

The control gain of an inverter is defined as the ratio of the peak value of the fundamental component in the pole voltage/phase voltage to the peak value of the modulating sine wave.

The control gain of an inverter, denoted by the symbol G is given by [8]:

$$G \equiv v_{A20,1}/v_{\text{mod}} = v_{A2N,1}/v_{\text{mod}}. \tag{4}$$

From the discussion presented in Section 3, it is evident that the proposed inverter scheme has the same control gain in both the operating modes.

For the 2-level inverter in the proposed inverter configuration, the control gain G is given by: $G = V_{dc}/2/2V_{cp}$, where V_{cp} is the peak value of the triangular carrier wave centered on O_2 (Fig. 2a).

Thus, multiplying the instantaneous values of modulating signals of the three phases (which is output by the controller) with the control gain G one may obtain the instantaneous values of

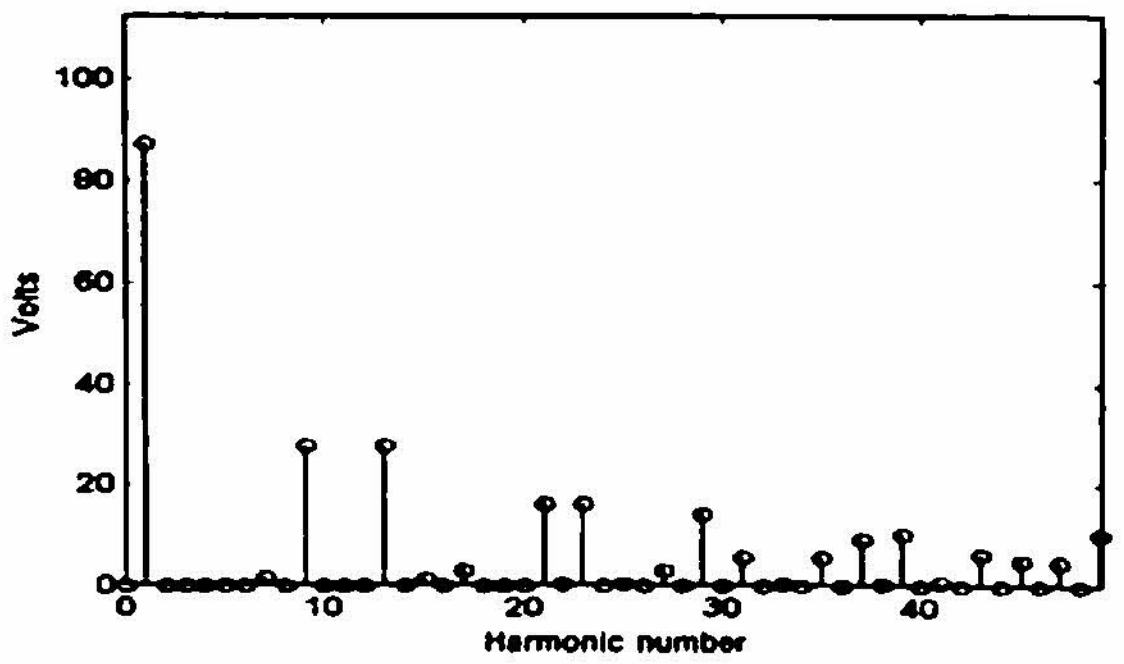

Fig. 2e. The harmonic spectrum of the motor phase voltage v_{an} at 2-level mode of operation on the verge of changing over to 3-level operation (refer Fig. 2b).

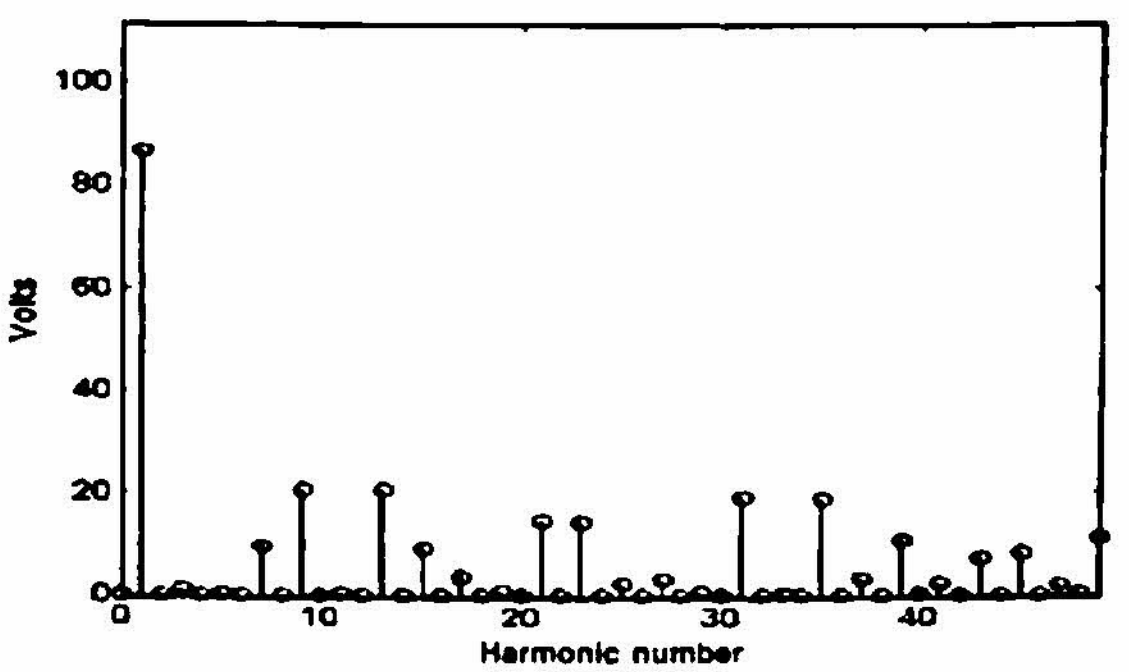

Fig. 2f. The harmonic spectrum of the motor phase voltage v_{an} at 3-level mode of operation on the verge of changing over to 2-level operation (refer Fig. 2c).

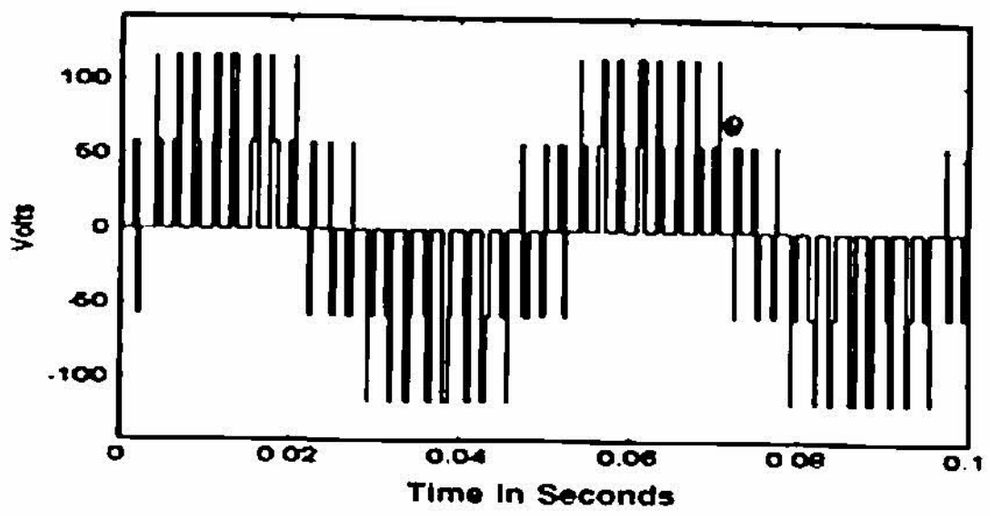

Fig. 2g. Simulated waveform of the phase voltage v_{A2N} in 2-level inversion mode (corresponding to the condition of Fig. 2a).

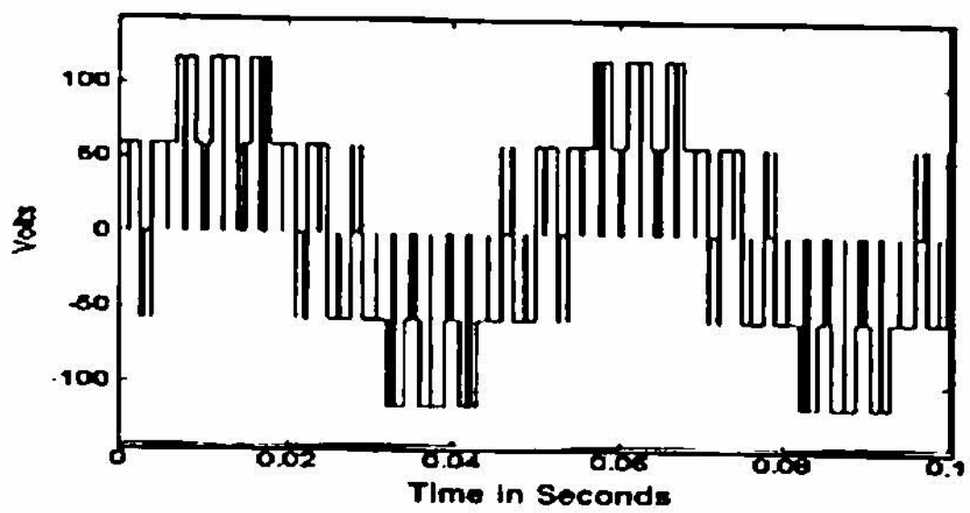

Fig. 2h. Simulated waveform of the phase voltage v_{A2N} in 2-level inversion mode which is on the verge of changing over to 3-level inversion mode (corresponding to the condition of Fig. 2b).

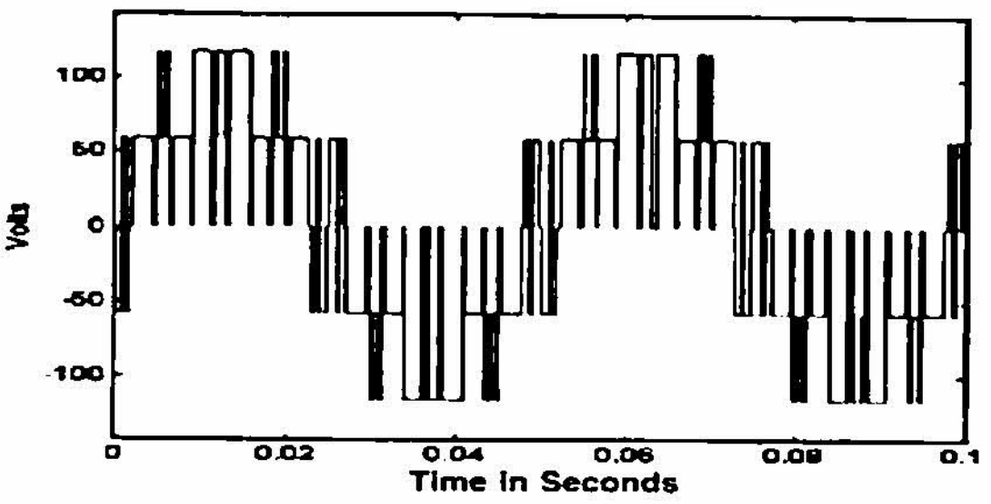

Fig. 2i. Simulated waveform of the phase voltage v_{A2N} in 3-level inversion mode (corresponding to the condition of Fig. 2c).

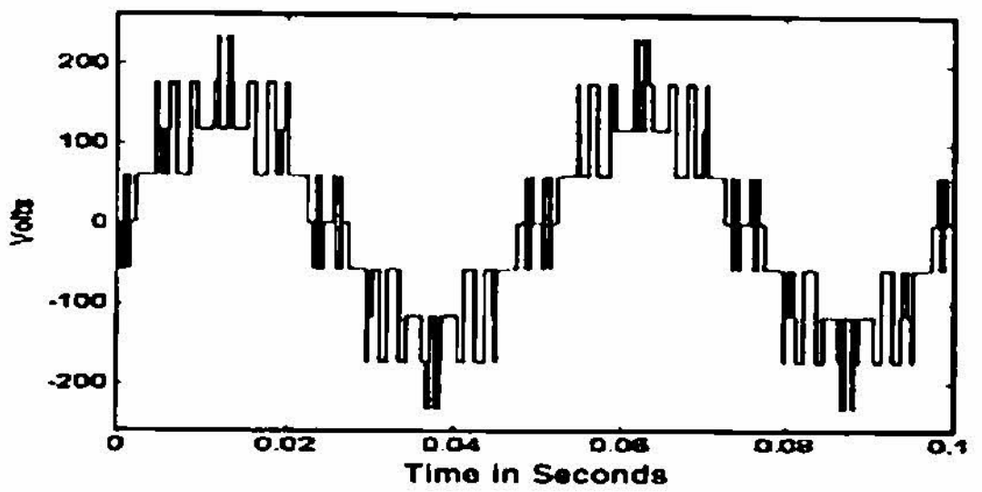

Fig.2j. Simulated waveform of the phase voltage v_{A2N} in 3-level inversion mode which is on the verge of changing over to 2-level inversion mode (corresponding to the condition of Fig. 2d).

the fundamental components of the pole voltages $v_{A20.1}$, $v_{B20.1}$ and $v_{C20.1}$, respectively. By using eqn (1), the spacevector $\mathbf{V_s}$ constituted by the instantaneous values of the fundamental components of the pole voltages $v_{A20.1}$, $v_{B20.1}$ and $v_{C20.1}$ may be determined. The required level of inversion (2- or 3-level) may then be determined by taking the modulus of the space vector. If $|\mathbf{V_s}| \leq \frac{\sqrt{3}}{4} V_{dc}$, the tip of the space vector $\mathbf{V_s}$ is situated within the inscribed circle of the inner hexagon, shown with a dotted boundary in Fig. 1b. This situation corresponds to the case of 2-level inversion. If the tip of the space vector is situated outside this boundary, i.e. if $|\mathbf{V_s}| > \frac{\sqrt{3}}{4} V_{dc}$, the situation corresponds to the case of 3-level inversion. Thus, the required level of inversion is identified.

Alternatively, the decision regarding the mode of inversion (2- or 3-level) can be taken based on the instantaneous values of the modulating sine waves output by the controller. As mentioned earlier, the symbol V_{cp} denotes the peak value of the lower triangular carrier wave centered on O_2 (Fig. 2a). Based on the control strategy presented in Section 3, the quantity 1.5 V_{cp} corresponds to the maximum length of the space vector, in the control domain, that can be realized in 2-level inversion mode (as the length of the space vector is 1.5 times the peak value of the modulating sine wave). Consequently, 2-level inversion is required if the length of the space vector constructed by the instantaneous values of the modulating sine waves is lesser than or equal to 1.5 V_{cp}. Else, 3-level inversion is required to construct the space vector defined by the instantaneous values of the modulating sine waves in the control domain. If the required level of inversion is three, the modulating sine waves corresponding to all of the phases are given a bias equal to the peak of the

lower triangular carrier wave centered on O_2 (Figs 2b and c). The PWM signals for the individual switching devices are then generated by comparing the modulating sine waves with the triangular carrier waves. Figure 3 illustrates the schematic block diagram of the implementation of the proposed SPWM strategy.

5. Performance of the proposed inverter in a closed loop system–a simulation study

For a further study of the performance of the proposed 3-level inverter in a closed loop system, simulation studies have been carried out for the speed control system of an induction motor under vector control. In this scheme, the proposed 3-level inverter feeds the three-phase induction motor. The dynamic performance of the induction motor is improved by employing a vector control scheme, compared to the scalar control schemes such as V/f control. In a vector control scheme, the flux and the torque dynamics of the induction motor are decoupled as in the case of a separately excited DC motor. Hence the dynamic performance of an induction motor under vector control is on par with that of a separately excited DC motor.

In vector control, the stator current of the induction motor is resolved into two orthogonal components, i_{mr} and i_{sq} in a synchronously rotating reference frame, popularly known as the 'd–q' reference frame in the literature. Also, the d-axis of the synchronously rotating reference frame is always aligned with the axis of the rotor flux under all dynamic conditions [9]. It may also be noted that the control is in the d-q frame of reference. Hence, all the reference and feedback quantities in this control system are DC quantities.

Of these two components, i_{mr} represents the magnetizing current along the axis of rotorflux and i_{sq} the component orthogonal to i_{mr}. The component i_{mr} causes the rotor flux and the component i_{sq} produces the torque. As the components i_{mr} and i_{sq} are orthogonal to each other, the torque

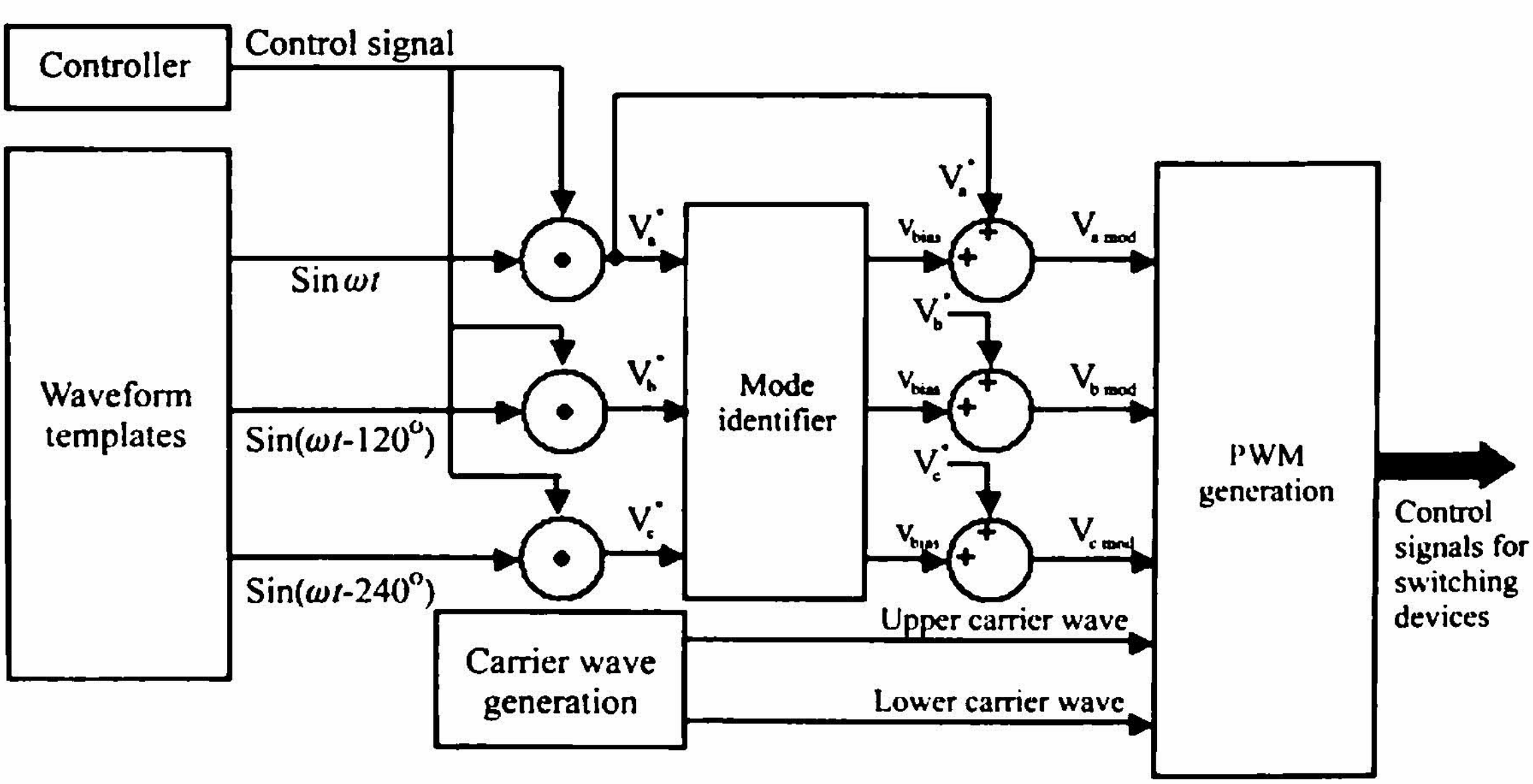

Fig. 3. Implementation of the modified SPWM scheme for the proposed 3-level inverter (v_{bias} = 0 in 2-level inversion mode and v_{bias} = peak value of the lower carrier wave in 3-level inversion mode).

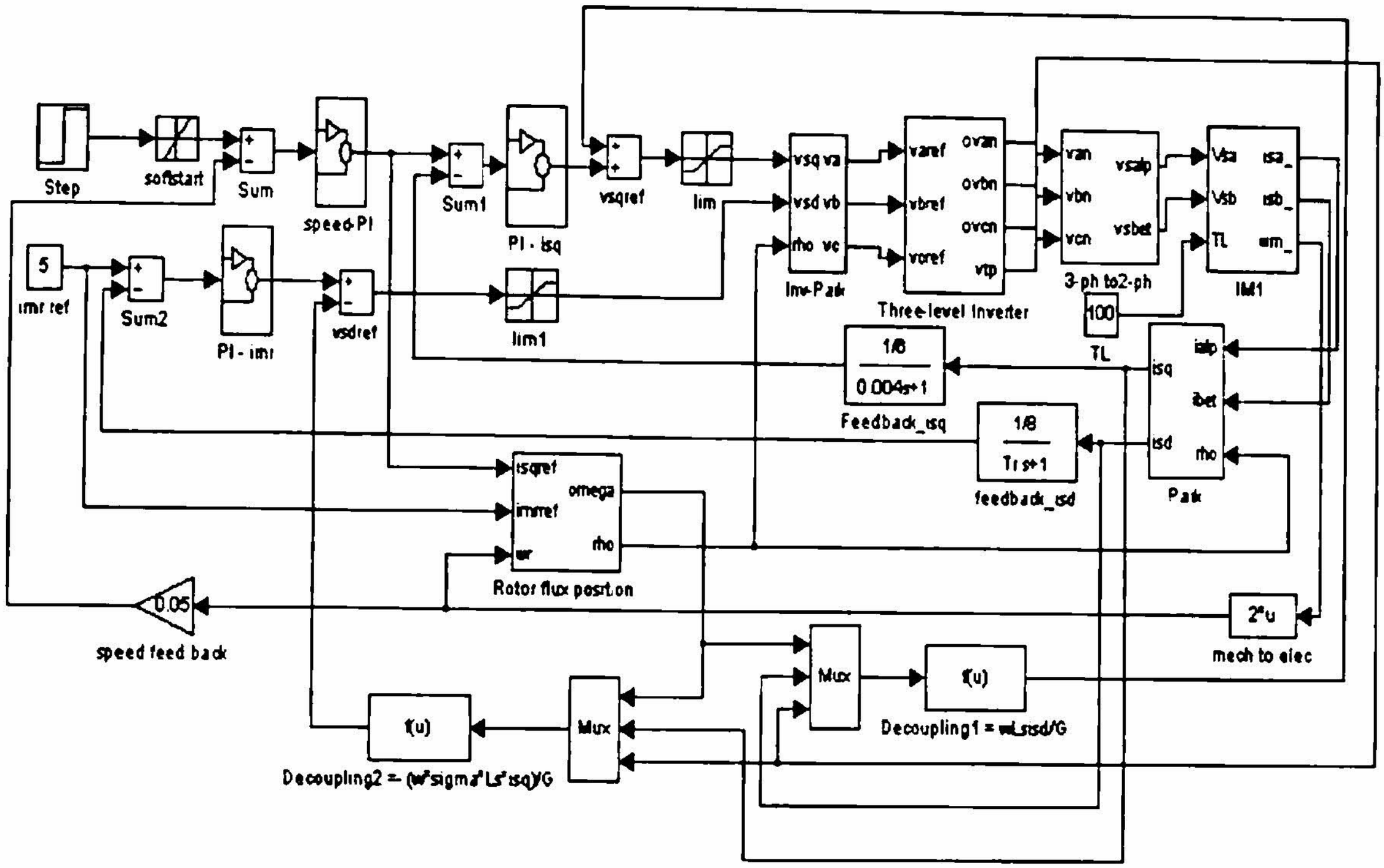

Fig. 4. Schematic block diagram of the vector control of induction motor employing the proposed 3-level inverter in Simulink.

dynamics and the flux dynamics are decoupled as in the case of a separately excited DC motor [9].

Figure 4 illustrates the model of the closed loop system of the vector control scheme, which employs the proposed 3-level inverter scheme. A constant flux operation is realized, as the reference for the magnetizing current in the d–q reference frame, denoted by i_{mr}^{*}, is a constant.

The error signal due to the deviation of the speed of the motor from the reference is amplified by the speed controller (which is a PI-controller), which determines the torque to be developed by the motor. Hence the output of the speed controller is the desired value of the torque-producing component i_{sq}^{*}.

In the closed loop system, the actual motor phase currents are sensed and the corresponding values of i_{mr} and i_{sq} are computed. The actual values are then fed back to the controller. The error between the reference value of the torque-producing component of the stator current i_{sq}^{*} and the actual value i_{sq} is amplified by a current controller (Fig. 4). Similarly, the error between the reference value of the flux-producing component of the stator current i_{mr}^{*} and the actual value i_{mr} is amplified by another current controller (Fig. 4). The output of the current controllers is then used to generate the modulating signals for the proposed 3-level inverter.

As the stator current components i_{mr} and i_{sq} are decoupled, the output of current controllers can be used as reference values for the current source inverter. However, in the case of a voltage source inverter, the stator voltage reference signals are not decoupled. Hence, suitable decoupling

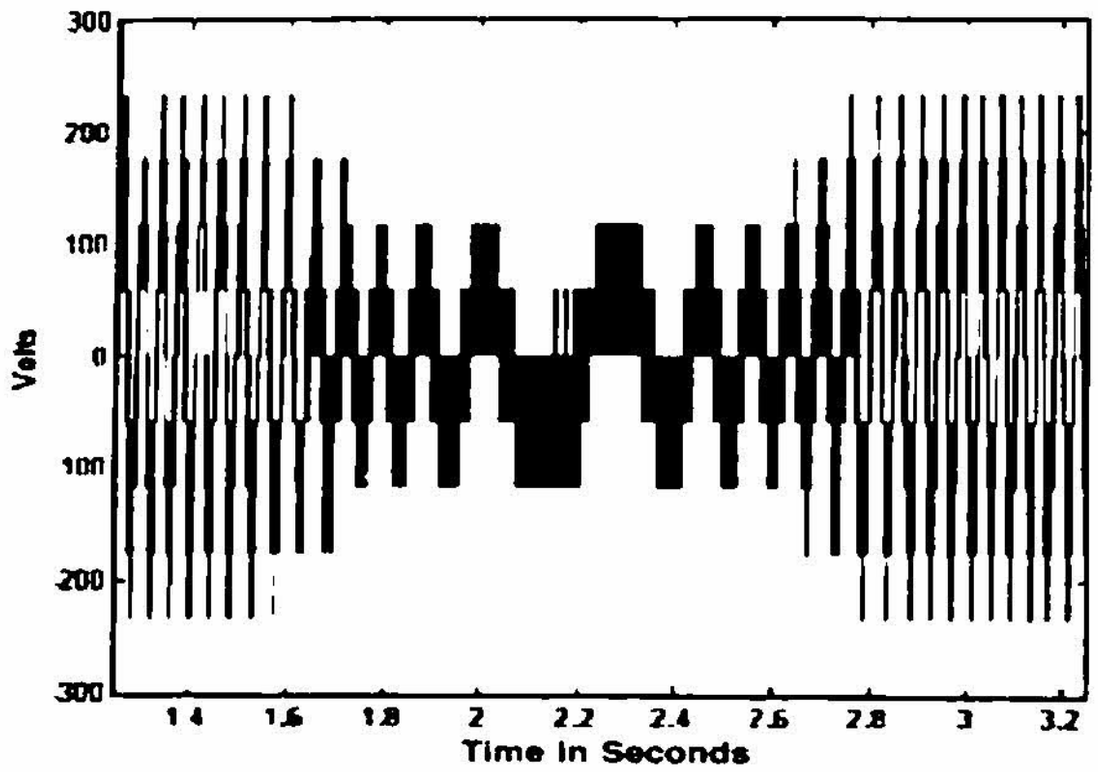

Fig. 5a. The motor phase voltage during speed reversal of induction motor under vector control employing the proposed inverter scheme. The figure shows a smooth changeover from 3 - to 2-level inversion mode and vice versa.

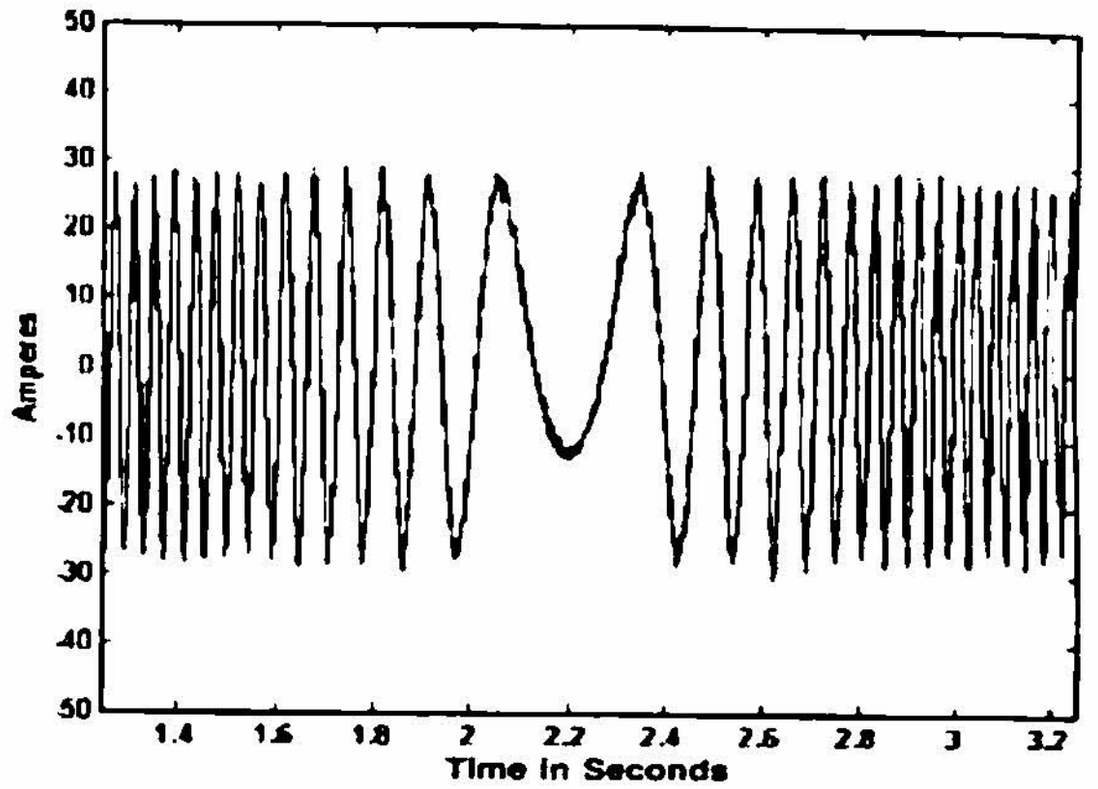

Fig. 5b. The motor phase current during speed reversal of induction motor under vector control employing the proposed inverter scheme.

terms are added to the output of the current controllers to generate the decoupled voltage reference signals [10] (Fig. 4).

Figure 5a presents the simulated voltage transient in the output phase voltage of the proposed 3-level inverter during speed reversal. It may be seen that the phase voltage changes over smoothly from 3- to 2-level inversion mode and vice versa while decelerating in the positive direction and then accelerating in the negative direction. Figure 5b presents the simulated motor phase current during this transition. It may be noted that the motor current too changes over smoothly with regeneration during the changeover. Figure 5c illustrates the simulated voltage transient when the load torque is given a step change from a no load to full load and vice versa. Similarly, Fig. 5d presents the simulated phase current transient during this period. It may be noted that a step change in the load-torque manifests emphatically in the phase current waveform but the phase voltage waveform remains relatively unaltered. Figure 5e presents the torque developed by the motor during this transient.

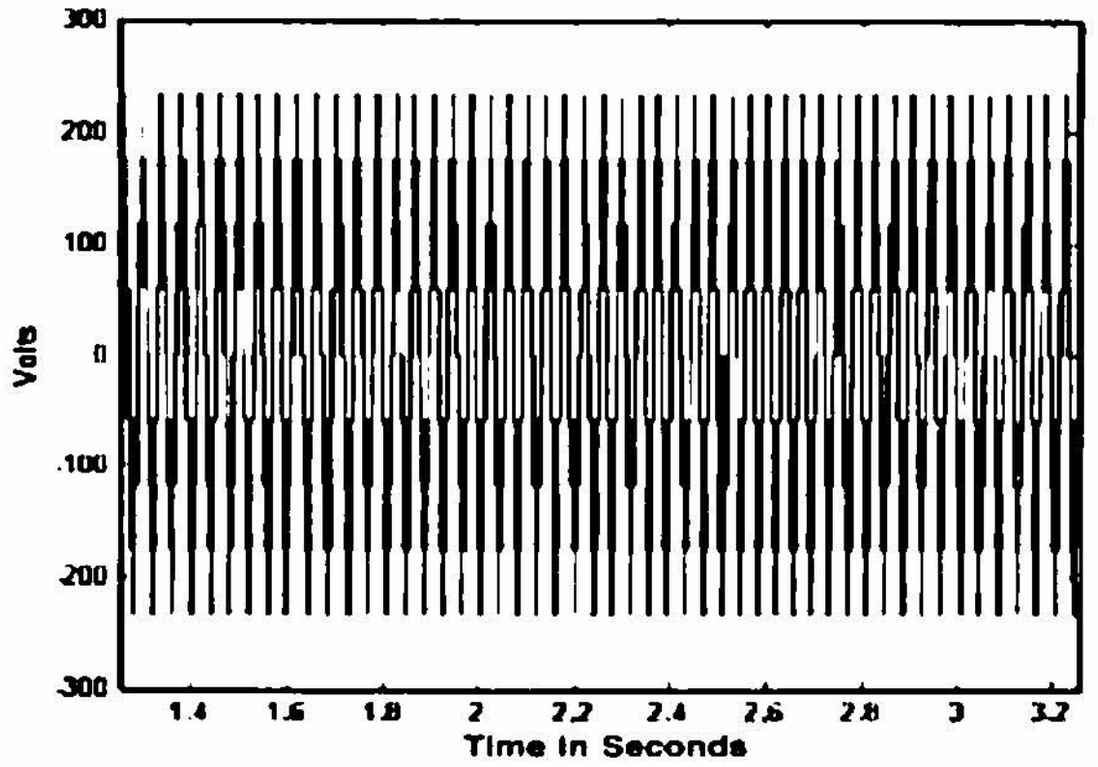

Fig. 5c. The motor phase voltage when the induction motor is suddenly loaded and unloaded under vector control employing the proposed inverter scheme.

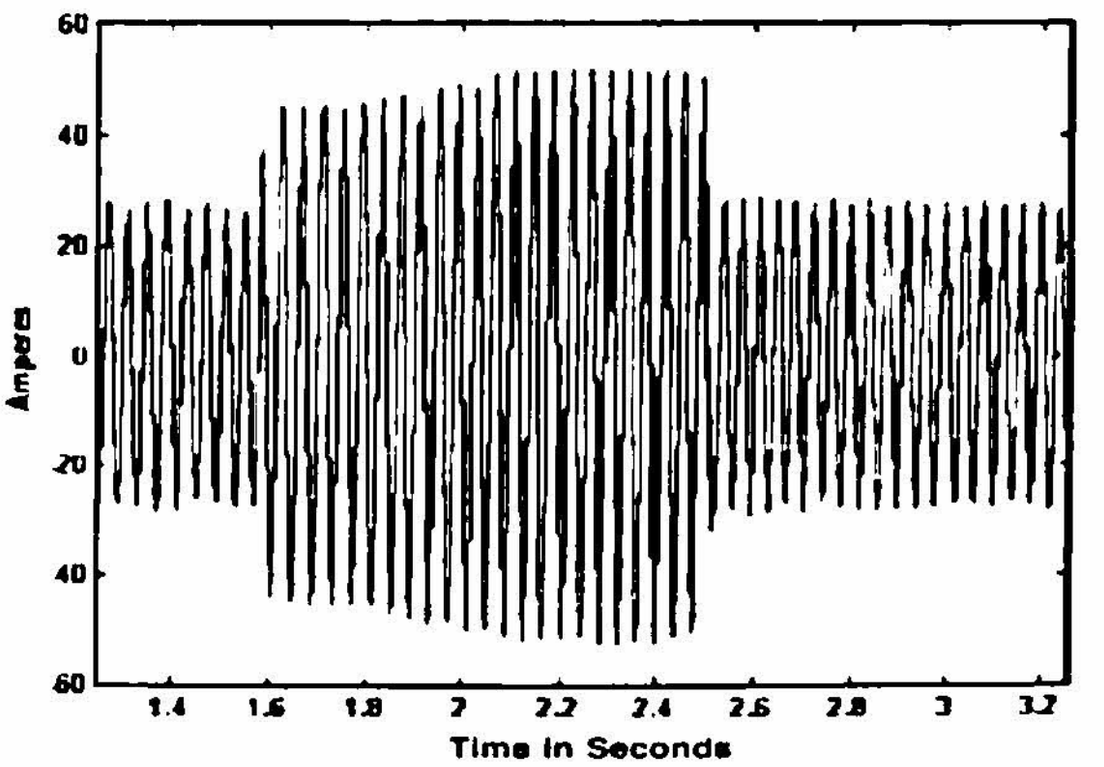

Fig. 5d. The motor phase current when the induction motor is suddenly loaded and unloaded under vector control employing the proposed inverter scheme.

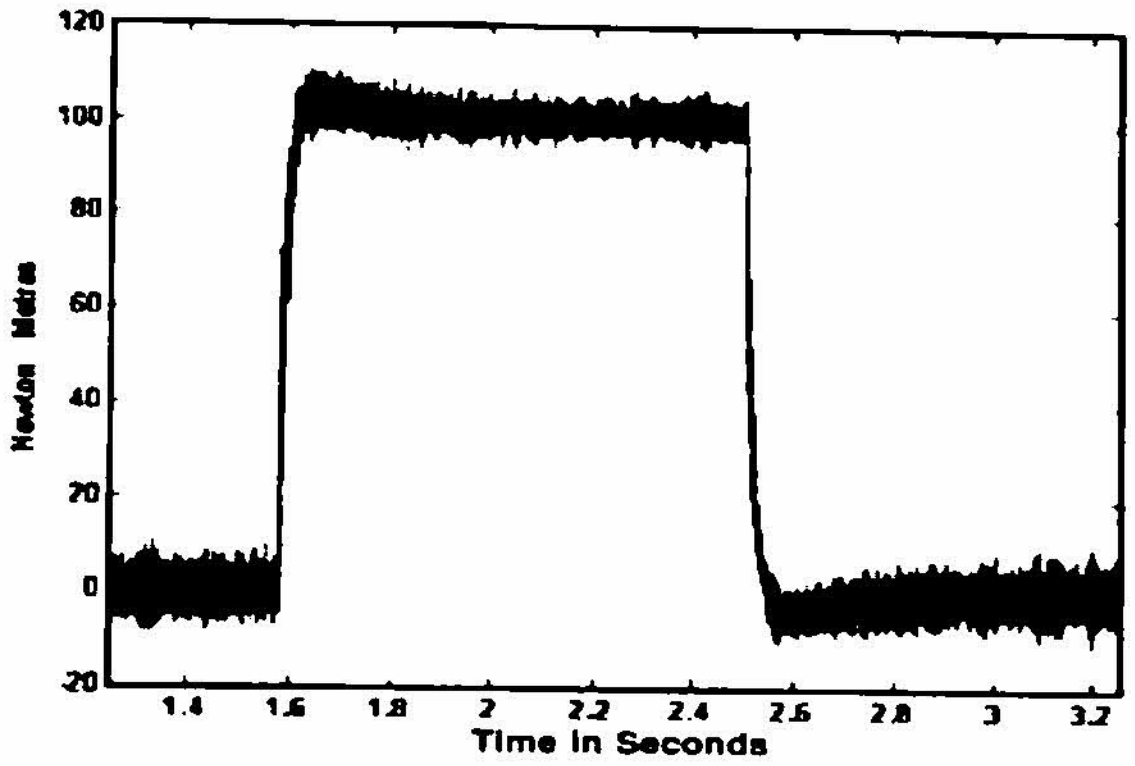

Fig. 5e. The motor torque developed when the full load is applied to the motor and then removed corresponding to Figs 5c and d.

From the above simulation results, it may be concluded that the proposed 3-level inverter is capable of rendering good performance with the proposed PWM technique.

6. Conclusions

The salient features of the proposed scheme are:

- A new 3-level voltage source inverter, obtained by cascading two 2-level inverters, is proposed in this paper. The DC link capacitors of individual inverters carry only the ripple currents and not the load current. Hence the voltage fluctuations of the neutral point are avoided in the proposed scheme.
- This configuration needs two isolated power supplies unlike its H-bridge counterpart, which requires three. However, three switches in the proposed scheme must be rated to block the entire DC bus voltage.
- In the lower range of output voltage, 2-level inversion can be achieved by switching only one inverter and therefore the switching losses are lower when compared to a conventional 3-level inverter.
- A modified sine-triangle-based PWM is also presented in this paper. The scheme is capable of ensuring a smooth changeover from 2- to 3-level inversion mode and vice versa.
- Experimental results are presented in open-loop condition. Simulation results indicate that the proposed inverter scheme is capable of rendering good performance in closed loop applications also.
- The application domain for this inverter is the same as that of the conventional 3-level inverter.
- This scheme may be extended to higher number of levels also.

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