AN ANNOTATED BIBLIOGRAPHY ON THRESHOLD LOGIC

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Received on July 24, 1976

ABSTRACT

With the advent of LSI technology and the dstl gate, the interest in threshold logic, which was extensively studied in the early 1960s, has been renewed. Winder had reviewed the various contributions in this area in 1959. This paper serves as a guide to the various contributions on threshold logic since 1959, to date.

Keywords: Adaptive and learning systems, artificial intelligence, Chow parameters, digital summation threshold logic (dstl) gate, information retrieval, k-acyclicity, k-comparability, k-summability, k-asummability, linear programming, linear inequalities, multigate synthesis, multivalued threshold logic, pattern recognition, probability transformation, pseudo-threshold logic, threshold gate, threshold logic, threshold decoding, monotonicity, variable threshold threshold logic, unate function.

In the early 1960's, Threshold Logic, the theory of threshold gates which have a higher information processing power than conventional gates, was extensively studied. However, a threshold gate requires components with close tolerances for its proper functioning. With the advent of LSI technology [1] and the dstl gate [2] it is possible to fabricate reliable threshold gates commercially [3, 4]. A competitive, compatible integrated threshold gate now exists with noise immunity superior to and tolerance requirement comparable with conventional gates. Hence the interest in threshold logic has been renewed. Winder [5, 6] had reviewed the various contributions in this area in 1967 and 1969. The present paper critically reviews the contributions since 1959 and will be hopefully useful to the various workers in this area.

Since the late 1950's, there has been a great interest in a class of switching functions which has been studied under different names such as threshold functions, linearly separable functions (LS functions), majority decision functions, setting functions, linear input functions, 1-realizable functions (realizable functions), voting functions, and STE (Single Threshold Element) realizable functions. Conventional gates like AND, OR and NOT are special examples of a threshold gate. A single threshold gate can represent a wide variety of complex switching functions, with a change of its structure. The principal goal of research in this area is the problem of devising a simple test and realization procedure for a given switching function to be realized as the output of a single threshold gate. So far, several methods for testing and realization of threshold functions have been developed.

A switching function of n variables is a threshold function if and only if a certain set of 2^n simultaneous linear inequalities in $(n+1)$ unknowns is solvable. The solution, if any, gives the weights and a threshold which realize the function.

Motzkin-Schoenberg [7] have presented a classical method of solving a system of linear inequalities by successive elimination of the various weights. McNaughton [8] offers a method of reducing the number of inequalities by identifying maximum false and minimum true vertices. Cobham [9] has investigated the simplification of a set of linear inequalities with (0, 1) coefficients. The boundary matrix and the boundary points of a threshold function, both of which correspond to the smallest irredundant set of inequalities, have been studied by Mays [10] and Fisher-Dearholt [11, 12] respectively. Sheng [13, 14] has presented a method in which the set of linear inequalities involving the weights of the variables is expressed in terms of the least weight and other incremental weights. A simpler set of inequalities is derived which is then solved through an ordering of the different incremental weights to provide information regarding 1-realizability and on the assignment of weights for realization, often without trial and adjustment). Sheng and Hwa [14-16] have generalized this secondary ordering method to yield a more general, more systematic and mathematically more rigorous procedure where a search for successively higher ordering is made. The given function can be partially specified. Further, Roy and Choudhury [17] have found that a number of incremental weights, large or small, depending on the given function, are equal. If a check is made to see which incremental weights can be made equal, the problem becomes simpler because of a smaller number of unknowns.

Choudhury, Sarma and Das [18] have shown that the entire set of inequalities can be classified into nine distinct types. The set of inequalities is next expressed in terms of the least weight and other different incremental weights. These two together provide information on 1-realizability and the minimal integer realization. Others who have presented algorithms for solving a set of linear inequalities are Agmon [19], Carver [20], Chang [21], Dines [22], Lee [23], Ho-Kashyap [24], Hu [25], Kuhn-Tucker [26], Mengert [27], Nagaraja-Krishna [28] and Warmack-Gonzalez [29].

Einhorn [30], Minnick-Einhorn [31], and Muroga, Toda and Takasu [32], use the simplex algorithm of linear programming to obtain solutions of the set of inequalities. Hu [25], has proposed the solution by Lemke's dual simplex method which is a variation of the simplex method.

Akers [33] applies the game theoretic approach to reduce the problem of 1-realizability to that of determining the value of a two-person, zero-sum game. Singleton [34] employs the matrix-theoretic approach, to solve the basic set of inequalities. Stram's [35, 36] profile technique is a practical method for realizing threshold functions by hand calculation. An n increases these methods are not suitable for hand calculation.

Torng [37] has developed a map method for testing and realization of threshold functions. The given function does not need any pre-processing such as positivizing and ordering.

Gaston [38] presents a simple test for linear separability but does not determine the weights required for separation. One advantage of his test is that if non-realizability is indicated, it is relatively obvious what coding changes will produce a realizable separation.

McNaughton [8] has shown that every threshold function is unate. Paull and McCluskey [39] have shown that unateness and 1-monotonicity are equivalent concepts. Winder [40, 41] has made a thorough study of complete monotonicity and has presented an efficient algebraic-logic test and synthesis procedure for the realization of threshold functions. Moore [42] and later Gableman [43] have disproved that complete monotonicity is sufficient for 1-realizability. However, for $n \le 8$, complete monotinicity is sufficient for 1-realizability. Fontao [44] has presented a graphical method for checking complete monotonicity. The observation of Muroga, Toda and Takasu [32] that the bias of a threshold gate can be treated like an input resulted in the concept of dual-comparability which was generalized into dual k-monotonicity by Liu [45, 46]. The concept of hypermonotonicity, due to Winder [47], unifies these ideas into one theory. Yajima and Ibaraki [48] who have extended this idea further, and also Liu [45] have given simple procedures for checking complete monotonicity.

The fact that 2-monotonicity determines ordering relations amongst the weights can be used to reduce the number of inequalities. Elgot [49] and Winder [40, 41] have presented methods for solving this reduced set of inequalities by eliminating one variable at a time. Gableman [43, 50] has given a trial method for solving the reduced set of inequalities.

The equivalence of complete monotonicity and 2-acyclicity has been established by Elgot [49]. For about an year, acyclicity, a concept of historical importance, was thought of as being a sufficient condition for 1-realizability. However, this has been disproved by Winder [41]. Another concept of historical importance is '*k*-unifinicity' [9]. It can be shown that *k*-unifinicity is equivalent to *k*-comparability and hence *k*-unifinicity is a necessary but not always a sufficient condition for 1-realizability. The function tree approach of Coates-Lewis II [51, 52], Coates-Kirchner-Lewis II [53] and Lewis II-Coates [54, 55] for testing and realization of threshold functions is computationally simple. The given function can be partially specified.

Winder [41] introduced the concept of 'asummability'. Elgot [49] has shown that a function is 1-realizable if and only if is asummable. Ghosh, Bandyopadhyay, Mitra and Choudhury [56] give simple algorithms for testing 2-summability by giving due consideration to the weights of the different minterms. These ideas can be easily extended for the testing of higher order asummabilities whenever desired. A faster method has been given by Sarje [57] which does not require the formation of all possible pairs of true and false minterms. An interesting relationship between 2-monotonicity and 2-asummability has been derived which leads to a much faster algorithm for testing 2-asummability. Further, an interesting conjecture on 'surface minterms' leads to a fast 2-asummability testing algorithm. Hopcroft and Mattson [58] have presented a method for checking 2-summability of switching functions by using decimal numbers for the vertices of the *n*-cube on which the function is defined. Bargainer and Coates [59] have improved the method so that m-summability can be checked. Roy [60] has given a test for 2-summability which uses the decimal numbers corresponding to the minterms of a function, a slide rule like device and a preformed chart. The device may be used for functions of upto six variables. Recently, Sureshchander [61] has presented a simple algorithm to check m-asummability. Also relevant are Cobham [62, 63] which are of limited value.

Biswas [64] has presented a computer programmable method for testing 1-realizability based on a comparison of the 'canonical composition structure' of the function under test with a standard table. The given function need not be completely specified. Sarje [57] has later improved on this method wherein a handy geometric structure, called the Implied Minterm Structure, enables one to test 2-monotonicity and conveniently identify threshold functions of upto six variables. In both these methods, pre-processing of the given function is required. Two heuristic procedures for manual computation of realization have been presented.

Dertouzos [65, 66] has presented a method in which a certain non-linear functional $I(\vec{c}, \vec{b})$ is minimized by an iterative approach. If $I(\vec{c}_0, \vec{b})$ 0, then the given function is realized by $\vec{c}_0$. Conversely, if $I(\vec{c}_0, \vec{b}) > 0$, then the given function is not 1-realizable. This procedure is useful when the number of variables is not large and we get only approximations to the desired weight-threshold vector. Also relevant are [67, 68].

Dertouzos [65, 66] has developed a procedure for perturbing any given vector of $(n+1)$ dimensions in such a manner that the distance between the given vector and a desired weight-threshold vector, if at all such a vector exists, is reduced. Thus, if the given switching function is 1-realizable, then the procedure will eventually yield an acceptable weight-threshold vector. If, on the other hand, the given switching function is not 1-realizable, the iteration process will eventually enter a limit cycle. Kaszerman [69, 70] has also discussed a similar iterative procedure developed from different viewpoints.

Dertouzos [65, 66, 71] has presented an expedient method, based on a concise tabulation of the canonic characteristic vectors of threshold functions. If a given function is 1-realizable, the method also provides the weight-threshold vector that is optimal in the minimum integer sense. The number of variables should not exceed six. Earlier, Chow [72] had found a set of $(n+1)$ parameters to uniquely characterize the realization of n-variable threshold functions. These parameters, called Chow parameters, have been extensively studied [73, 74]. In so far as threshold functions are concerned, either the Chow parameters or the Dertouzos's characteristic vector contain equally all the necessary information. However, in the tabulation of threshold functions, the use of the characteristic vector provides a more economical representation.

Winder [75] has compared seven methods for deriving approximate realizing weights and threshold for a threshold function, the Chow parameters being given. He has established a certain geometric rule as the best.

A switching function f is a threshold function if and only if there exists a hyperplane which separates all the true vertices of f from all the false vertices of f. For $n \leq 4$, the conventional geometric representation allows immediate determination of whether or not a given function is a threshold function. A necessary and sufficient condition for a switching function to be a threshold function in terms of convex hulls has been given by Highneyman [76].

Liu [45] has used Triquare maps to test and realize threshold functions. The given function needs no pre-processing and may be partially specified. Its usefulness does not decline rapidly when it is used to solve problems beyond six variables.

The methods due to Blomgren-Torng [77], Dodd [78, 79], and Gonzalez [8.] are somewhat limited. Wong-Eisenberg [81] have presented a special iterative algorithm for the realization of threshold functions. Others who have studied the testing and realization of threshold functions are Baugh [82], Butakov [83], Cheney-Hu [84], Chow [85], Fischler [86, 87], Goto [88], Hrùz [89], Hu [25, 90], Hurst [91] Krohn-Rhodes [92], Lee [93] Muroga [9, 94, 95], Opferman [96], Roy [97], Sarma [98], Sha-Sze [99] and Varshavski [100].

One way of realizing a non-threshold function is by means of a multi-threshold threshold gate (MTTG). Whereas a threshold gate has a single threshold, an MTTG which is a generalization of the threshold gate has more than one. Spann [101] has discussed λ-threshold realizability of an arbitrary function of n variables in terms of Rademacher-Walsh coefficients. A list of structures for multi-threshold threshold gates with the minimum sum of integral weights was prepared by Haring and Ohori [102]. The minimality of the number of thresholds, however, is not guaranteed. Synthesis procedures of structures for multi-threshold threshold functions have been discussed by Ercoli-Mercurio [103], Ghosh [104], Ghosh-Choudhury [105, 106], Haring [107], Haring -Diephuis [108], Lieb-Muroga [109], Liu [110], Mow-Fu [111], Necula [112], Sethares [113], Sethares-Pierce [114], Sheng-Roy [115], and Yen [116, 117]. Yen's [116, 117] method is based on integer programming. One of Haring's [107] synthesis procedures is based on the synthesis method of Coates and Lewis II [55].

Another way of realizing switching functions which are not 1-realizable is by means of a network of threshold gates inter-connected in a suitable manner. Compound synthesis of threshold gate network is the realization of any arbitrary function with a number of threshold gates. The problem of compound synthesis of any function using feed-forward paths only has been studied by many authors. As a physical device, a threshold gate has certain limitations such as the number of inputs, the magnitudes of the weights and threshold value, the tolerance of the weights and threshold value, etc. Networks of threshold gates can be studied in the light of these considerations. Amarel, Cooke and Winder [118], Cohn and Lindman [119], Horna [120], Lindaman [121], Muller and Winder [122], Miyata [123], Rudeanu [124], and Tohma [125] have studied majority gate networks with a fixed number of inputs. Lewis II and Coates [55, 126] and Coates and Lewis II [55, 127] have studied networks of threshold gates with a specified tolerance on weights and threshold value.

Miyata [123] has presented a simple straight-forward and systematic method for synthesizing three input majority gate networks. Although the optimal network is not obtained, a network with fairly few gates rest lts. This method can be extended to the synthesis of networks composed of five input or seven input majority gates.

Aker's [128] method of realizing functions with three input majority gates involves the construction of a logically passive self-dual or LPSD. Horna [129] has proved that Aker's method is unable to lead to the minimal network in many cases. Negrin [130] has modified Aker's method so as to minimize gating and delay elements. Riseman [131] has also modified Aker's method wherein a more precise construction of the LPSD is presented and delay elements are reduced.

Hanson [132] has shown that algebraic methods are readily applicable to compound synthesis of three variable functions. Most of the resulting networks are minimal.

Horna [120] has generalized the geometric interpretation of switching functions and presented a simple method for the synthesis of any arbitrary logical network by three input majority gates.

Tohma [125] has presented methods for decomposing logical functions using 3 input majority gates. The decomposition method is based on the property of unateness. Rudeanu [124] has given general solutions of Tohma's equations in a more symmetric form and with shorter proofs.

Lindaman [121] has presented a theorem for deriving majority gate networks within an augmented Boolean algebra. Cohn and Lindaman

[119] have axiomatically developed an algebra suited to logical design with majority decision gates.

Miller and Winder [122] have studied majority gate synthesis by geometric methods based on intution and do not guarantee optimal solutions.

General compound synthesis without taking the physical limitations into consideration for symmetric functions has been studied algebraically by Kautz [133] and Roy [134, 135] and graphically by Sheng [14, 136].

Minnick [137] has developed techniques for the logical design of magnetic core circuits to produce any arbitrary switching function.

Hopcroft and Mattson [58] have presented an algorithm for synthesizing single and multiple output networks which realize switching functions, not necessarily completely specified, through the use of a minimum number of threshold gates.

Sarma, Das and Choudhury [138] present a method of decomposition of switching functions into unate functions for synthesis with threshold gates. Sheng [14, 139] has proposed a method of synthesis by decomposing any switching function into a sum or product of threshold functions.

Ghosh, Basu and Choudhury [140] have presented a decomposition and reconstruction approach for synthesizing any switching function. Attention is mainly focussed on cascade type realizations. Near minimal solutions are readily derived. This method has been successfully applied to functions of upto six variables.

Using the concept of 'admissible pattern', Dertouzos [65, 66] has presented methods for threshold-OR network synthesis and threshold cascade synthesis. Partially specified functions and multiple output networks can also be treated.

Dertouzos [66] has presented spectral methods for network synthesis where the characteristic vector is augmented with additional correlation coefficients to give what is called a spectra of 2^n real numbers.

Certain five operations in the Rademacher-Walsh transform domain give rise to a very concise method of classifying switching functions. This method of classification has been used by Edwards [141] to synthesize completely specified switching functions of single output systems in an elegant way by using a universal threshold logic gate.

Breur [142], Cameron [143], and Muroga-Ibaraki [144], have discussed the synthesis of an optimum network by integer linear programming. The linear programming approach developed by Minnick [137] and Einhorn [30] employs the simplex method with artificial variables and can be used to synthesize a network of threshold gates.

Hughes [145] has presented a computer programmable algorithm for the design of general feed-forward networks of threshold gates. A simplified version of the algorithm is presented for the case of symmetric functions. The case of partially defined functions is also treated.

Using the profile technique, Stram [36] has presented a method of compound synthesis by deleting some true vertices and then by ORing together the outputs of reduced and auxiliary functions.

Using higher-order monotonicity, Winder [41] has presented efficient methods for compound synthesis. The resulting network need not be optimal.

Yajima and Ibaraki [146] have used the concept of 'mutual monotonicity' to compound synthesis. Although the method is heuristic and does not yield an optimal network, the resulting network is fairly economical. This method can be used for hand computation for functions of upto seven or eight variables. Incompletely specified functions can also be treated. The multiple output problem can also be treated.

Yau and Ostapko [147] have presented a simple and economical method for the compound synthesis of a class of switching functions called threshold product functions. Ostapko and Yau [148] have also presented a method for realizing any arbitrary switching function with a 2-level network of threshold and parity elements.

Liu [45] has used Trinquare maps for compound synthesis. Don't care cases can also be treated.

The geometrical concept of 'region' or 'connectedness' is a weak but easy-to-visualise necessary condition for 1-realizability which is far from being sufficient for 1-realizability. However, the region concept has been used by Kaszerman [149] for the synthesis of two threshold gate networks

Hrùz [89] has presented a method to check whether a given switching function is unate from the truth table of the function. One of his two methods of synthesis utilizes the concept of 'transition of argument' and the other method utilizes the concept of 'code distance'. Both the methods lead to minimal or near to minimal networks.

Carroll and Coates [150] have dealt with the synthesis of two-level network of threshold gates for realization of non-linearly separable functions. The realization obtained contains the minimum number of threshold gates possible for a 2-level realization. The given function may be partially specified.

Ali and Ahmed [151] have applied complementary even parity functions to the synthesis of non-threshold functions.

Srivatsa-Biswas [152] have developed a test procedure for threshold functions of upto 6 variables with the help of a Karnaugh map. No resort to the inequalities has been made. It has been shown that linear separability of a unate switching function corresponds to 'compactness' of the plot of '1's on the various cells of a Karnaugh map. If non-realizability is indicated, it is relatively obvious what coding changes will produce a realizable separation. Next, an algorithm has been presented to synthesize a non-linearly separable switching function with the minimum number of threshold gates connected in cascade. Partially specified functions can also be treated. The algorithms presented are suitable for hand calculation, no pre-processing of the given function is required and the final result is obtainable in short time. No new algorithm to find the weight-threshold vector of a 1-realizable function directly from its plot has been given. The tables of Dertouzos [66] are used for this purpose.

Others who have studied compound synthesis are Aida [153], Akers-Robbins [154], Breeding [155], Butakov-Bykova-Vorob'ev [156], Choudhury-Sarma [157], Cooper [158], Fischler [86], Fischler-Tannenbaum [159], Hopcroft [160], Hu [25], Kashyap [161], Krohn-Rhode [92], Mattson [162], Meo [163], Muroga [164], Nechiporuk [165, 166], Pratapa Reddy [167], Raship [168], Sha-Sze [99], Stabler [169], Varshavski [170], Winder [171], and Zakharova [172].

The generation of all threshold functions of exactly n variables from all threshold functions of exactly $(n - 1)$ variables has been studied by Muroga [173], Dertouzos [66], Winder [174], and Ishii-Kimura [175]. No efficient method of generation is known.

The classification of threshold functions has been studied by Goto-Takahasi [176] Dertouzos [66], Liu [45], and Winder [177] and their enumeration by Muroga [178, 179], Winder [174, 180], Dertouzos [66], and Deanholt [181].

The general problem of how many threshold functions there are for n variables remains unsolved at present. An upper bound on the number of threshold functions with n variables was derived independently by Cameron [182], Perkins-Willis-Whitmore [183], and Winder [41]. Theoretically interesting lower bound, which is not particularly useful, was obtained independently by Dahlin [9], Smith [184], and Yajima-Ibaraki [185]. Also relevant are [186, 187].

Wills [188] has disproved Elgot and Muroga's [189] conjecture that the minimum set of weights are always integers. In the worst case, the necessary size of weights increases at least exponentially with n [9, 176, 190] Bounds on the magnitude of a weight have been studied by Goto [191] and Muroga [9, 192]. The upper bound on each optimum weight has been investigated by Muroga-Toda-Takasu [32], Muroga-Toda-Kondo [178], Winder [174, 180] and Muroga-Tsuboi-Baugh [179]. Optimum structures for threshold functions of 8 or fewer variables have been obtained by Muroga-Tsuboi-Baugh [179].

The upper bound on the number of required threshold gates for an arbitrary switching function has been studied by Muroga [9, 193], Nechiporuk [166] and Haring [107] and in particular for symmetric functions by Kautz [133]. The lower bound has been investigated by Cameron [182], Winder [194] and Nechiporuk [166]. Specific optimal realizations of each type of four argument function have been enumerated in Minnick [137], Cyprus [195], and Tsuboi [196] (Optimal realizations using 3 input or 5 input majority gates).

The reliability of a threshold gate has been discussed from different viewpoints [14, 55, 66, 197]. The digital summation threshold logic (dstl) gate, proposed by Hurst [2, 198], has a higher reliability than the analog summation threshold logic (astl) gate, this being achieved at the cost of higher gate complexity and propagation delay. Pratapa Reddy [167, 199] has critically studied and modified Hurst's dstl gate so as to reduce gate complexity and propagation delay.

Multi-valued threshold logic has been studied by many authors [200–209]. Variable threshold threshold gates were studied by Meisel [201–212].

Dertouzos [66] has stressed the need for finding and studying stochastic threshold logic. Timevarying threshold logic was investigated by Nelson, Daly and Joseph [213]. Strongly asymmetric threshold functions have been studied by Muroga [9, 173]. Threshold functions of order r have been studied by many authors [214–219]. An extension of threshold logic was studied by Slivinski [220, 221]. A single number, named degree of separability, which Slivinski [220, 221] introduced, can not only tell us whether a given switching function is a threshold function, but also whether it is a pseudo-threshold function, a quasi-threshold function or some other. Others who have studied pseudo-threshold logic are Baugh [222], Breeding [155] and Fagerlin [223].

Conventional arithmetic circuits can be easily realized using threshold gates. A large number of networks were devised by Japanese in the course of their research on parametron computers and electronic telephone exchanges in the mid-1950's. For most of the networks, it is difficult to determine who should be given credit. Fischler [87] and Fischler-Poe [224] have presented circuits for adders, subtracters and complement generators. Others who have studied threshold realization of arithmetic circuits are Coates-Lewis II [225], Gustafson-Haring-Susskind-Willis [226], Hotz [227], and Winder [228]. Some of the practical implications of threshold logic were studied by Coates-Lewis II [229] and Muroga-Takoshima [230] by building the DONUT computer and MUSASINO-1 computer respectively. Threshold logic synthesis of sequential circuits has been studied by Hadlock [231], Hadlock-Coates [232], Masters-Mattson [233], and Meisel [211]. Logic hazards in threshold networks have been investigated by Howe and Coates [234].

Threshold logic is useful in simplifying reasoning about complicated networks, as for example, in the problem of minimizing the number of inverters in a network [235].

Threshold logic is one of the basic approaches used often in pattern recognition [219, 236–247] and artificial intelligence [248]. The use of threshold gates in the Perceptron has been studied by Widrow-Hoff [249] and in Adaline by Mattson [162]. Threshold decoding, which is a decoding method of a certain type of error-correcting code, was pioneered by Reed [250], and developed by Massey [251, 252]. The concept of threshold logic is studied with respect to information retrieval [253]. A threshold gate can be used as an error correcting device [254, 255]. One of the most important and promising fields of application of threshold gates is adaptive and learning systems [256, 257]. Sheng [14, 258] has shown that threshold gates can be conveniently and advantageously employed for probability transformation. Lastly but not the least, the theory of threshold principle has also been studied with respect to biological systems [259] and economies [260].

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