Nonlinear A/D converters: some new techniques

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Abstract

Nonlinear A/D converters are receiving wide attention from system and circuit designers. They can be applied to solve many problems of data acquisition and encoding in the field of instrumentation. Some new generalized techniques to implement these converters are presented in this paper.

Key words : Non-linear A/D converter, non-linear D/A converter, Haar function, iteration, cascade connection.

1. Introduction

Nonlinear A/D converters are a class of data converters which are useful in instrumentation, communication and other applications. In instrumentation many transducers have nonlinear characteristics. The use of nonlinear converters makes it possible to obtain a linear relationship between the digital output and the physical parameter. Digital communication systems, such as PCM require companding of speech signals to maintain a uniform signal/noise ratio over a wide dynamic range, which can be accomplished by means of nonlinear A/D converters. Also these converters are useful in generating nonlinear functions as required in signal processing systems.

2. Nonlinear A/D converters—A state of the art review

This field has received considerable attention in the past few years in view of the above applications and recent advances in IC technology. Several schemes have been developed for realizing nonlinear A/D converters, of which three important methods are described below. In one approach, a linear A/D converter is preceded by a nonlinear analogue converter. In another approach, the nonlinear converter is of digital type and it follows a linear A/D converter. In yet another approach, the nonlinear conversion and A/D transformation are performed by the same circuit which cannot be easily separated. In such a case, the A/D converter may be termed as composite nonlinear A/D converter. Important aspects of all these schemes are given below:

(a) Nonlinear A/D converter based on analogue converter

A block schematic of the converter is shown in Fig. 1. Some of these analogue converters employ the nonlinear V–I characteristic of certain electronic devices and perform nonlinear conversion. Junction diodes and transistors with collector shorted to base have been used to generate nonlinear functions. These are connected in the feedback or input network of an OPAMP to obtain logarithmic or exponential conversion[1]. The nonlinear transconductance of FET's has been exploited for implementing polynomial law conversion[2]. SCR's are also used to realize quasi-logarithmic function[3]. In this operation, the SCR acts as a feedback resistor for an OPAMP so that the quasi-logarithmic function is generated.

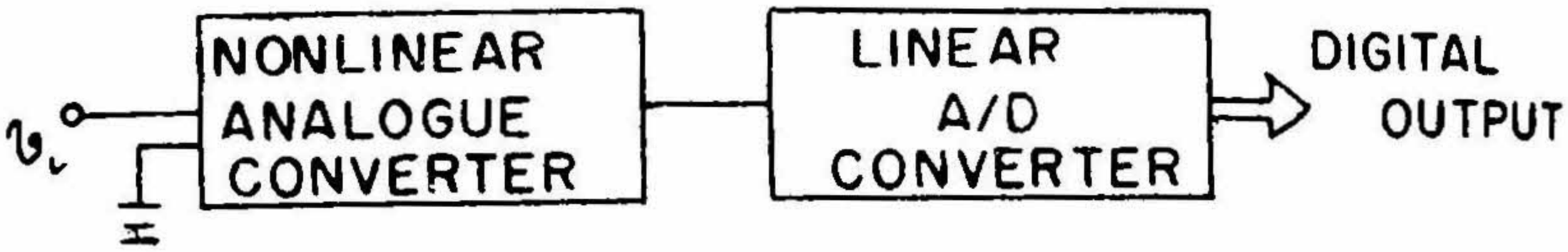

FIG. 1. Nonlinear A/D converter based on analogue converter.

A different approach for realizing nonlinear converters is based on the piecewise linear approximation of nonlinear functions. In this method, diodes and resistors are appropriately connected to generate the required function[4]. Another technique utilizes an analogue multiplier to implement square, square-root, polynomial and inverse functions[5]. These multipliers are available in IC form and have the desirable features of good linearity, wide bandwidth, low drift and low cost.

In general, it is relatively easy to implement this type of nonlinear converter. However, the disadvantages associated with these converters are limited accuracy, variation in circuit performance with temperature and ageing and device matching problems.

(b) Nonlinear A/D converter based on digital converters

As shown in the block diagram of Fig. 2, a linear A/D converter is followed by a nonlinear digital converter. Various numerical algorithms are available to implement digital converters[6, 7] as required in this application. Both sequential and combinational techniques are employed in these converters. An alternative approach makes use of nonlinear counters, whose outputs are nonlinear functions of the number of clock pulses fed into them[8]. The block diagram of a nonlinear A/D converter utilizing this counter is shown in Fig. 3. When the conversion is completed, both linear and nonlinear digital outputs are available at the respective output terminals of the counters.

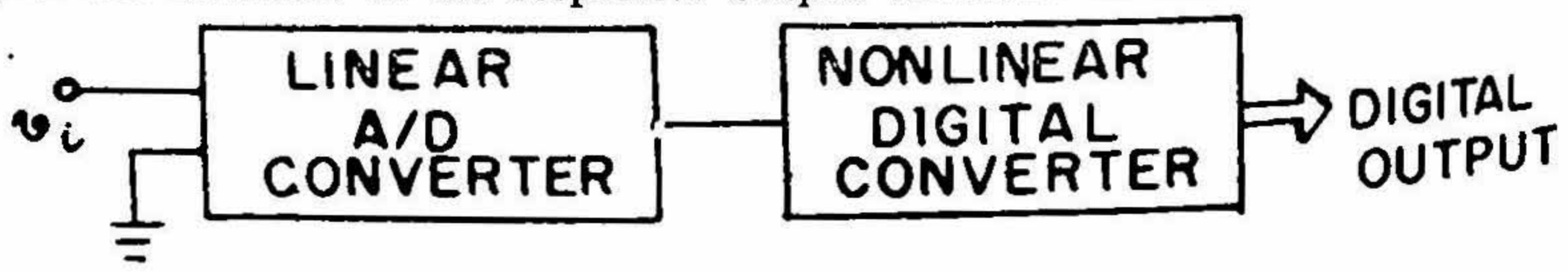

FIG. 2. Nonlinear A/D converter based on digital converter.

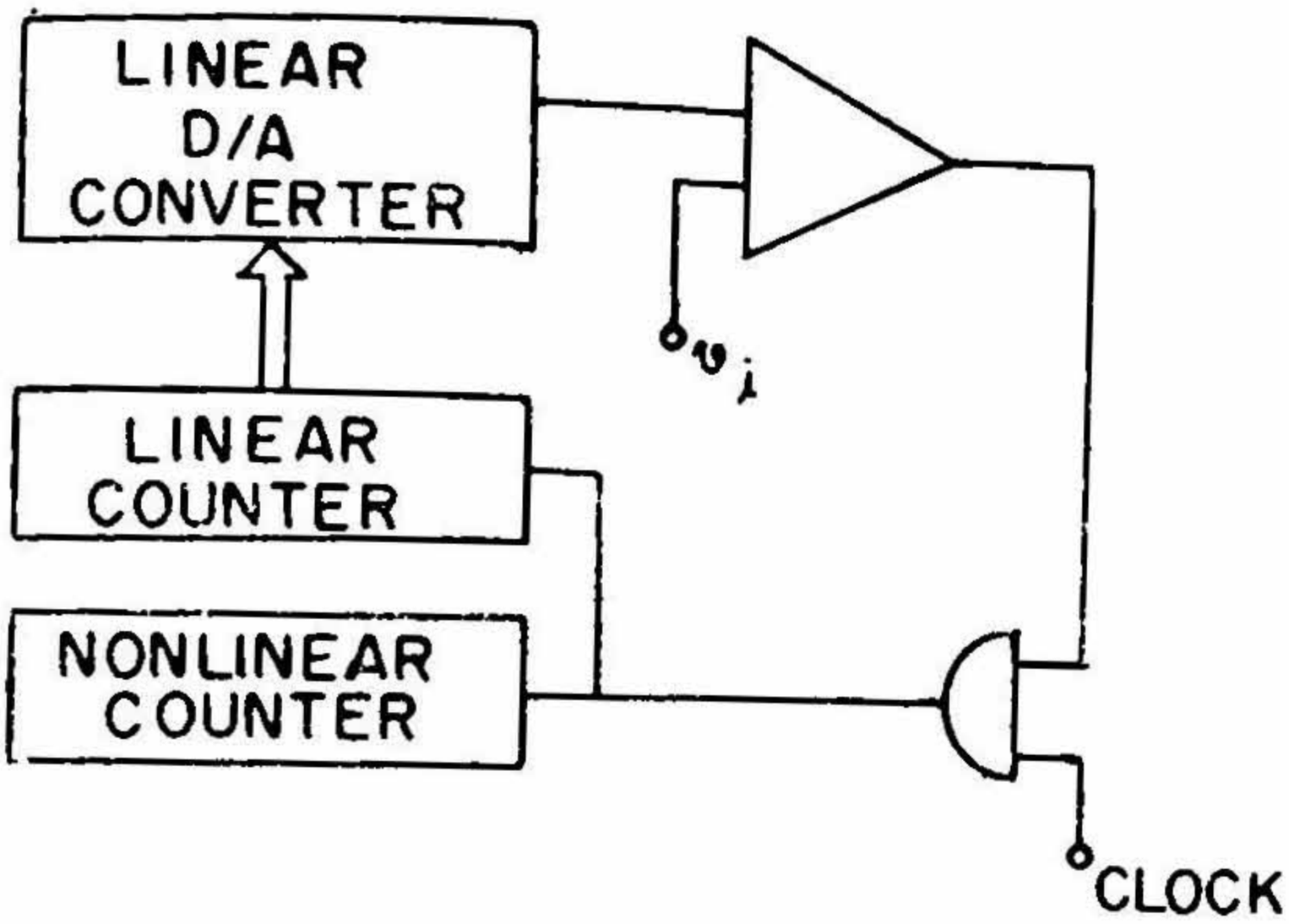

FIG. 3. Nonlinear A/D converter based on nonlinear counter.

The accuracy and resolution of this type of converter are essentially determined by the linear A/D converter. Therefore, the association of a nonlinear digital converter with this system, ensures that the same performance is maintained. The disadvantages associated with this system are its increased complexity and lower operating speed.

(c) *Composite nonlinear A/D converters*

Like linear A/D converters, these are also classified as 'open loop' type and 'feedback' type. Hence there are many possibilities for achieving nonlinear A/D conversion using this approach. Typical examples of 'open loop' type converters are logarithmic RC discharge voltage-to-time converter[7] and dual-slope type A/D converter[10]. In the former type, a capacitor is charged to an input voltage v_i and then discharged through a resistance. The dual-slope technique is utilized to realize logarithmic, polynomial, exponential, square-root and square functions. Important aspects of a polynomial converter following this approach are described below as a typical example.

Fig. 4 shows the schematic of a polynomial converter. The operation of this converter is very similar to that of the linear dual-slope converter. It is easy to see from Fig. 4 that the input-output relationship of this converter is given by,

$$v_i = at + bt^2 \tag{1}$$

where t represents the time period during which a reference voltage V_R, is connected to the integrator and a and b are constants. Since a and b are dependent on the values of R and C in the circuit, the value of t gets affected by their variations. This sets a limit on the performance of this converter.

The 'feedback' type of converters employ nonlinear D/A converters as feedback blocks in association with suitable logic circuits. The nonlinear D/A converters are

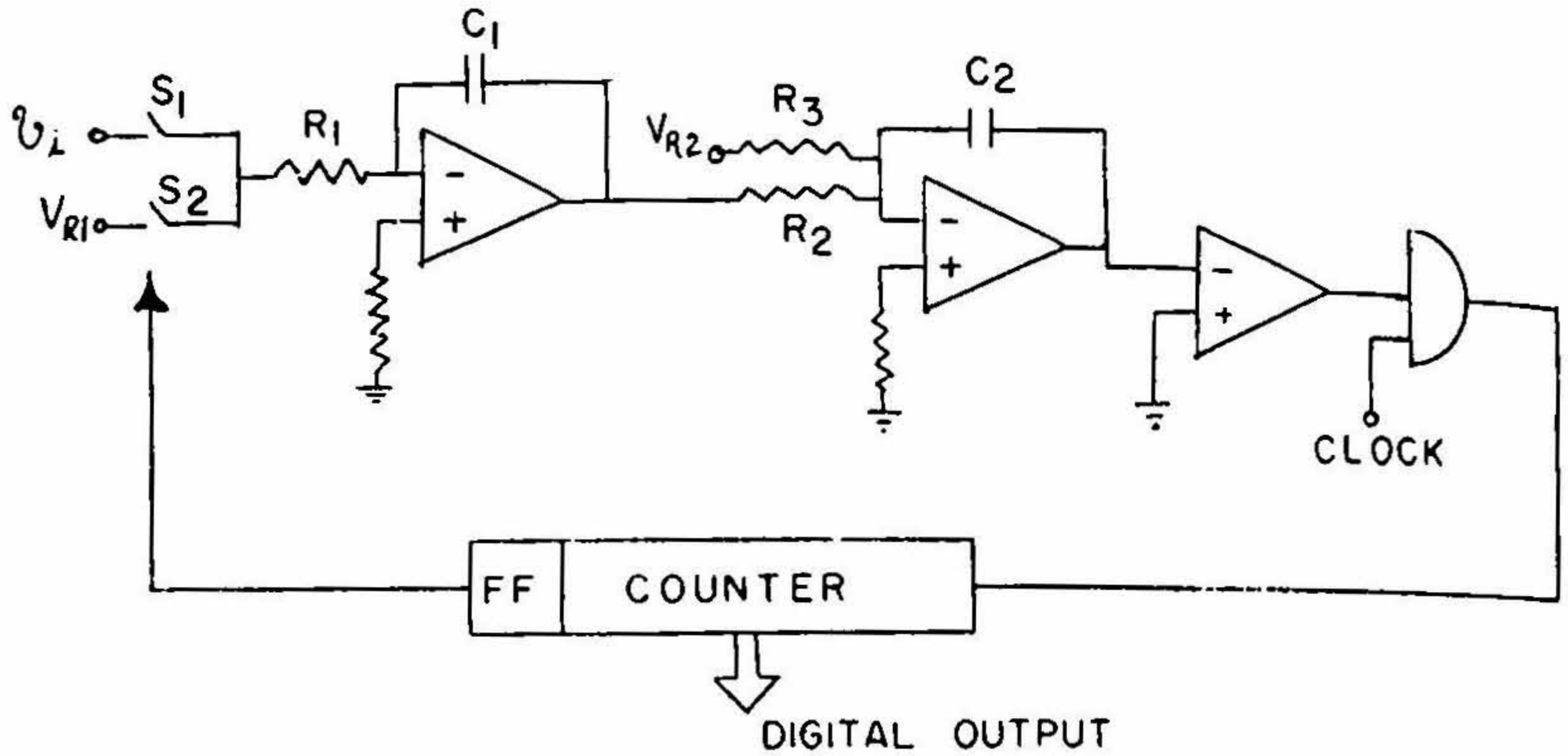

FIG. 4. Polynomial converter.

realized using a linear D/A converter in conjunction with a transcoder[11]. An alternate method in realizing nonlinear D/A converters employs resistors and analogue switches[12,13].

The A/D converters described above have low system complexity similar to those described in (*a*). Since their nonlinear characteristics are not dependent on the non-linear nature of any device, their resolution and accuracy are as good as those described in (*b*).

3. Some new techniques for nonlinear A/D converters

Important features of nonlinear A/D converters have been covered in the previous section. It is clear from the above discussion that no effort seems to have been made towards the realization of a generalized algorithm to implement nonlinear A/D converters. Hence it was decided to conduct a detailed investigation on nonlinear A/D converters. The result of this is the systematic synthesis of nonlinear functions and development of the following techniques for realizing nonlinear A/D converters:

(*a*) Conversion using Haar functions,

(*b*) Iteration, and

(*c*) Cascade connection of linear D/A converters.

These converters make use of nonlinear D/A converters as their feedback blocks. The block schematic of such a converter is shown in Fig. 5. It comprises a voltage comparator, control logic circuits, a counter, a nonlinear D/A converter, and a clock generator. The D/A converter is driven by the counter and its output voltage, v_0, is a nonlinear function of input digital data D. At the end of the conversion, v_0 equals the input voltage v_i. Thus

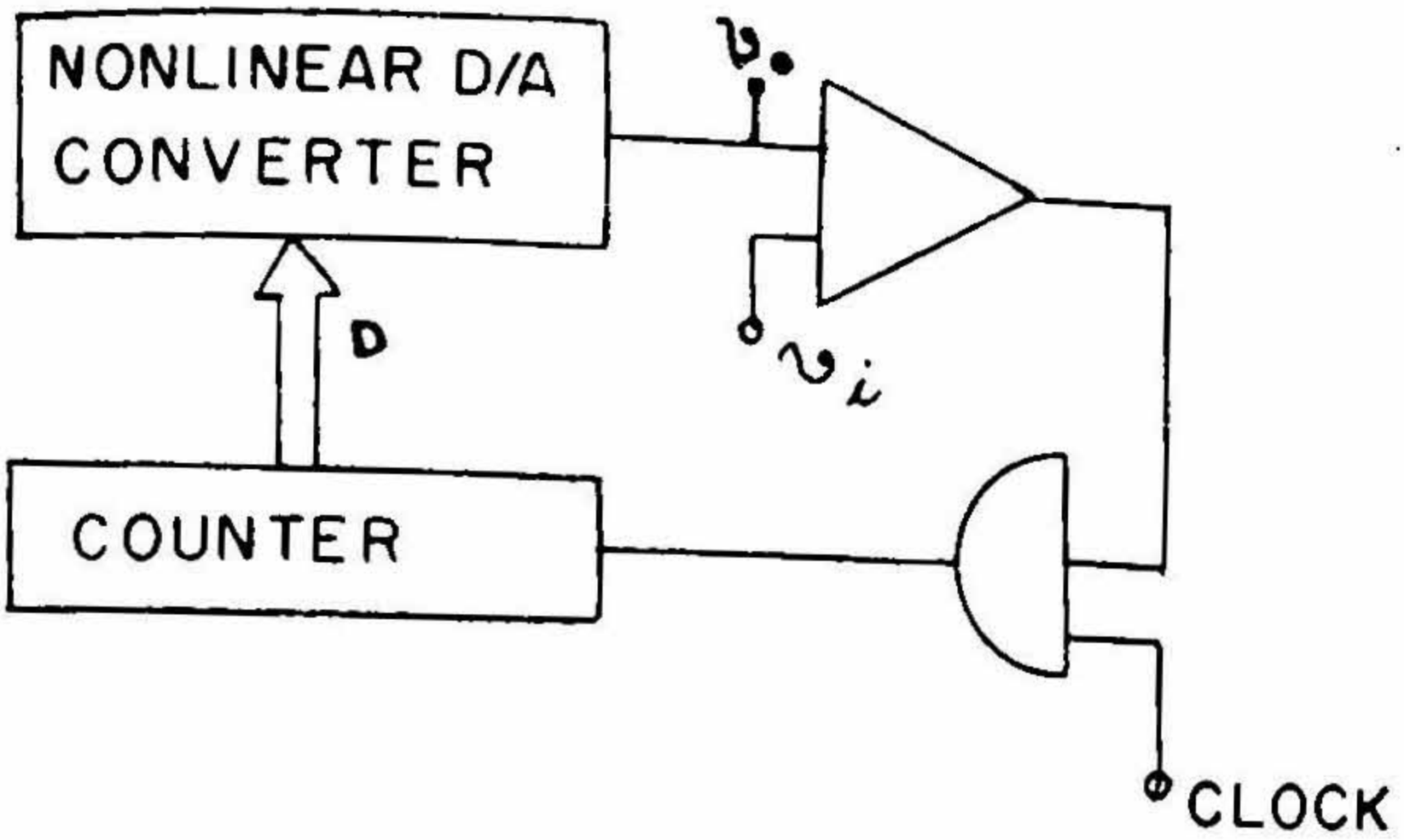

FIG. 5. Nonlinear A/D converter.

$$v_0 = f(D) = v_i \tag{2}$$

or

$$D = f^{-1}(v_i) \tag{3}$$

where

$$D = \sum_{i=1}^{m} a_i/2^i$$

with $a_1, a_2 \cdots a_m$ as digital inputs to the D/A converter. The different techniques to implement nonlinear A/D converters are described below in detail.

(a) *Conversion using Haar functions*

In this type of conversion, a nonlinear D/A converter based on Haar functions is utilized. The block schematic of a nonlinear D/A converter based on Haar functions is shown in Fig. 6. The digital input drives the Haar function generator. The Haar functions produced at its output are multiplied according to the required weights by the weight multiplier. The multiplied weights are added by a summing amplifier which produces the corresponding analogue voltage at its output.

The Haar functions are described by the following equation :

$$\begin{aligned} HAR\ (2^p + n,\ D) &= +\sqrt{2^p},\ n/2^p \leqslant D \leqslant (n + 1/2)/2^p \\ &= -\sqrt{2^p},\ (n + 1/2)/2^p < D \leqslant (n + 1)/2^p, \\ &= 0, \text{ elsewhere.} \end{aligned} \tag{4}$$

FIG. 6. Nonlinear D/A converter based on HAAR functions.

where $p = 0, 1, \cdots, n = 0, 1, 2 \cdots (2^p - 1)$ and D is the given variable. A continuous function $f(D)$ can be synthesized from a Haar series as shown below:

$$f(D) = \sum_{n=0}^{\infty} C_n \, \mathrm{HAR}\ (n,\ D) \tag{5}$$

where,

$$C_n = \int_0^1 f(D).\ \mathrm{HAR}\ (n,\ D)\ dD \tag{6}$$

The Haar functions can be derived from block functions which are defined by the following equation:

$$q\,(2^p,\ n;\ D) = \begin{matrix} 1,\ n/2^p \leqslant D \leqslant (n+1)/2^p \\ 0,\ \text{elsewhere} \end{matrix} \tag{7}$$

where $p = 0,\ 1 \cdots$ and $n = 0,\ 1 \cdots,\ (2^p - 1)$

The Haar functions can also be expressed as combination of positive and negative block functions as shown by the following equation:

$$HAR\ (O,\ D) = q\ (1,\ 0;\ D)$$

$$[HAR\ (2^p + n,\ D) = \sqrt{2^p}\,[q\,(2^{p+1},\ 2n;\ D) - q\,(2^{p+1},\ 2n+1;\ D)] \tag{8}$$

where p and n indicate the degree and the order of block functions respectively.

The block functions can be generated easily. The schematic diagram of a typical block function generator is shown in Fig. 7, which produces block functions corresponding to digital input. It consists of several binary-to-decimal decoders, driven by the digital input. The decoder I produces a_1 (MSB) and its complement. The decoder II has two digital inputs a_1, a_2 and produces four block functions, $q\,(4, 0;\ D) - q\,(4, 3;\ D)$. Similarly the decoder III has three inputs and it generates eight block functions, *viz.*, $q\,(8, 0;\ D) - q\,(8, 7;\ D)$. In general, a decoder M produces 2^M block functions.

The first block function is equal to '1' for the entire range $0 \leqslant D \leqslant 1$. The two block functions produced by decoder I are used to generate HAR (1, D). In a similar manner, HAR (2, D) and HAR (3, D) are produced employing block functions generated

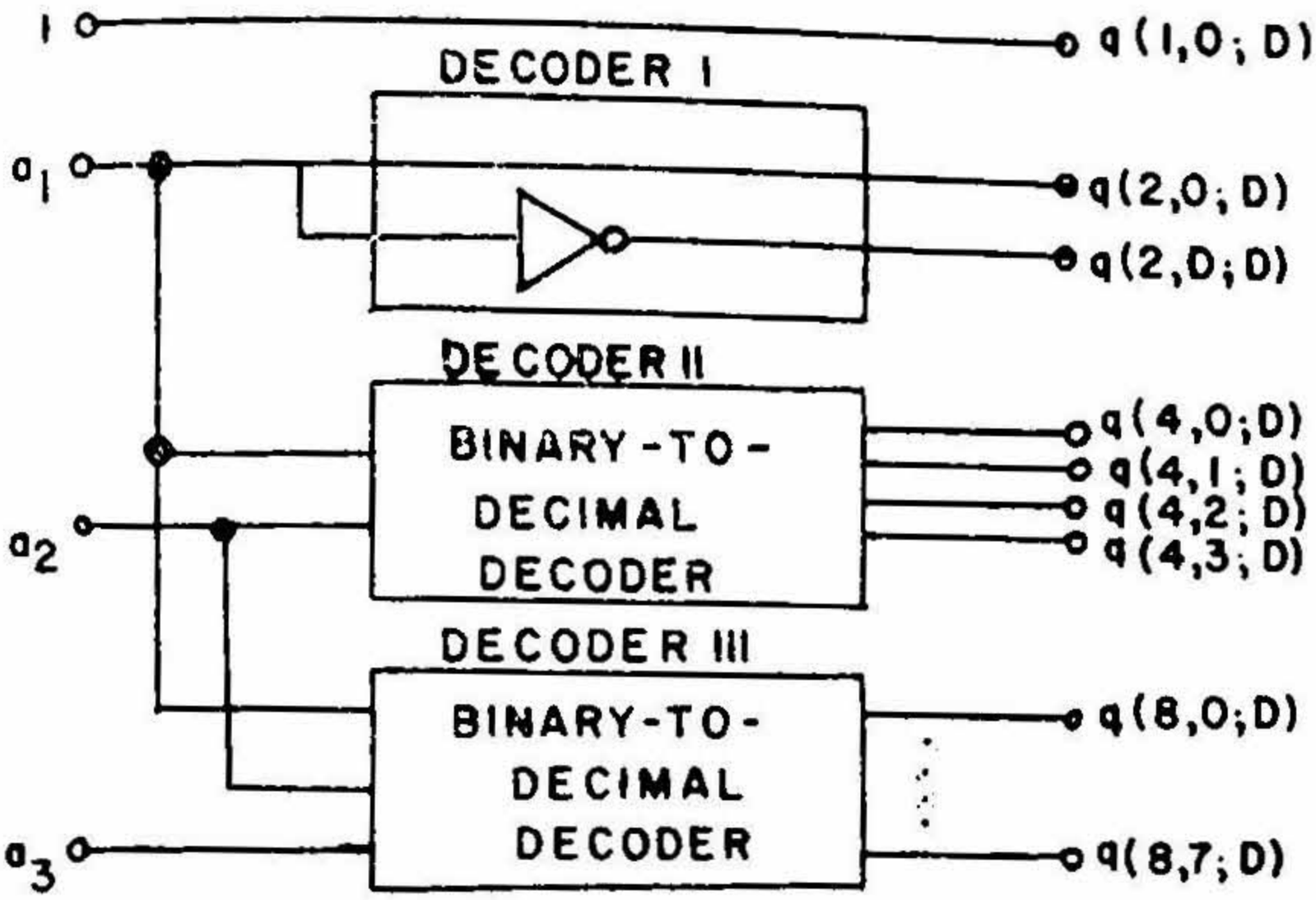

FIG. 7. Digital-to-block function generator.

by decoder II. The block functions of decoder III generate HAR (4, D) — HAR (7, D). Thus, an m-bit digital input can produce 2^m Haar functions. The schematic of a circuit to produce Haar functions from block functions is shown in Fig. 8. The three SPST switches S_1–S_3 facilitate the connection of reference levels $+V_p$, $-V_p$ and ground to the output terminal in response to the block function signals. When block function $q(2^{p+1}, 2n;\ D)$ assumes '1', $+V_p$ appears at the output. The succeeding block function $q(2^{p+1}, 2n+1;\ D)$ drives S_2 and $-V_p$ now appears at the output. When both are in 'O' state, the switch S_3 is turned ON connecting the output to ground. Thus the circuit produces HAR $(2^p + n,\ D)$.

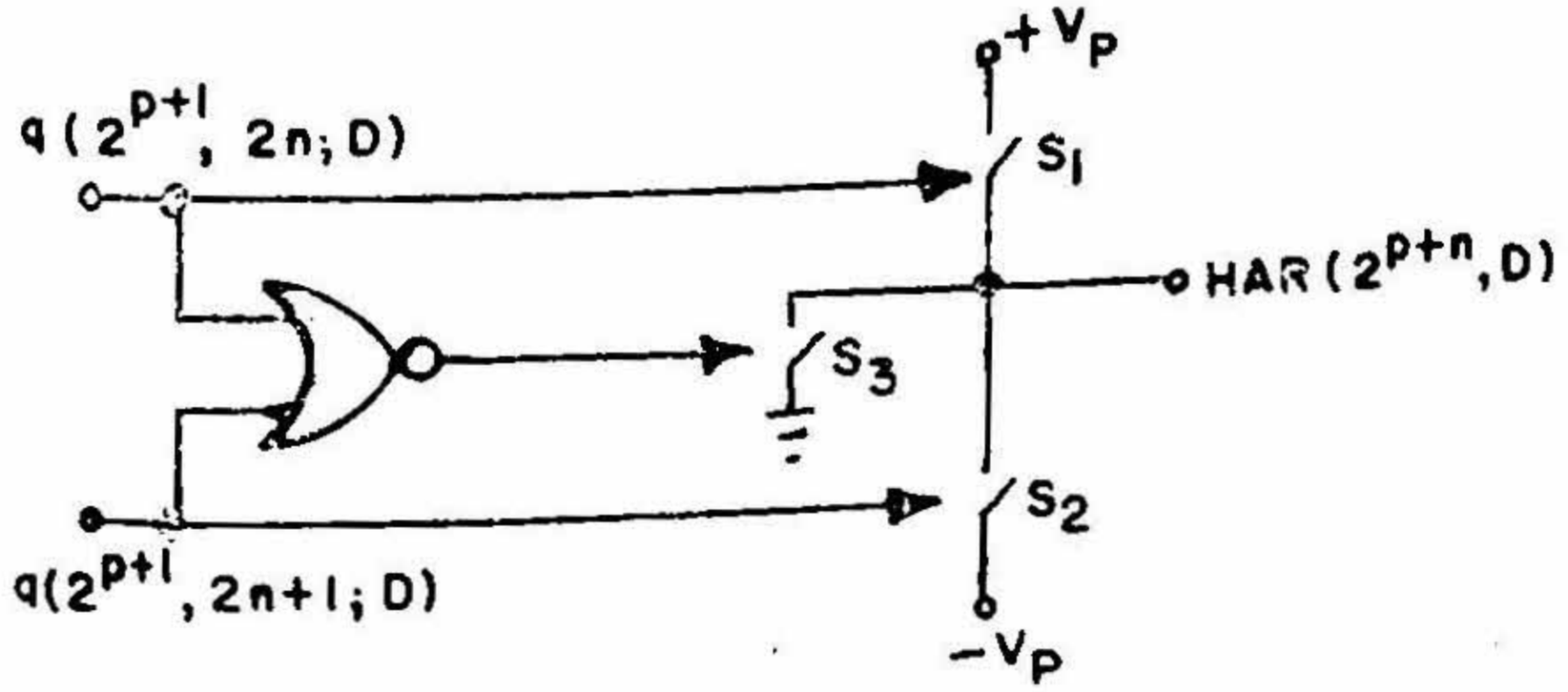

FIG. 8. Block function-to-HAAR function converter.

The Haar functions so produced have to be multiplied by weights C_n. The summing amplifier shown in Fig. 9 adds the input voltages in a proportion determined by the input

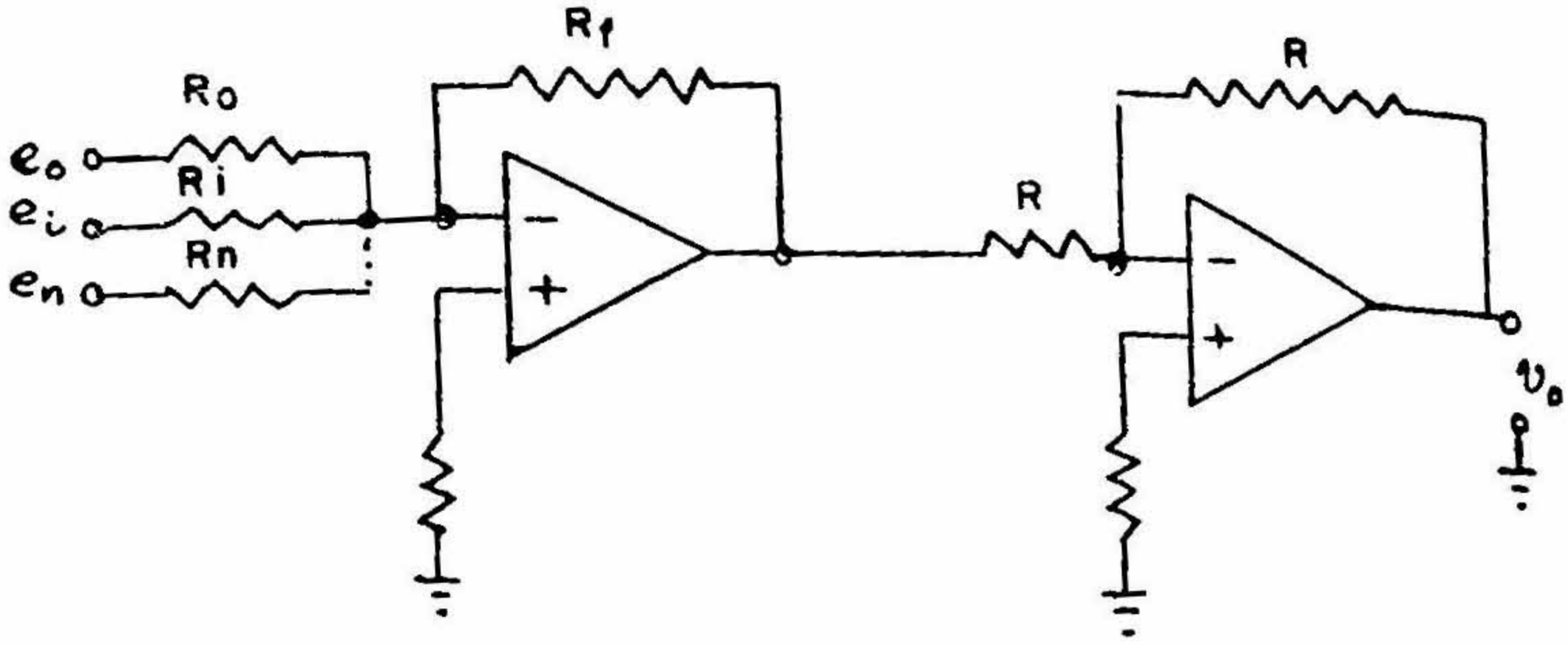

FIG. 9. Summing amplifier.

resistance network. The coefficients C_i are calculated for the given function. If C_i is negative, the polarity of the ith Haar function is reversed before feeding to the adder circuit. Let e_n be the voltage corresponding to HAR (n, D). Then,

$$v_0 = R_f \sum_{i=0}^{2^m-1} e_i/R_i \tag{9}$$

where, $R_i = 1/C_i$.

Hence,

$$v_0 = R_f \sum_{i=0}^{2^m-1} C_1 e_i$$

$$= R_f \sum_{i\ 0}^{2^m-1} C_i \ \text{HAR}\ (i,\ D) \tag{10}$$

Thus, a nonlinear analogue output voltage is obtained corresponding to the digital input. The conversion time of this D/A converter can be made very small by using a high slew rate OPAMP for the summing amplifier. This D/A converter can be employed in the feedback path of an A/D converter to realize appropriate nonlinear functions.

(*b*) *Conversion using iteration*

In this section nonlinear A/D converter based on iteration technique is presented. The main advantage of this system is the relatively low complexity of the hardware. In this method, a nonlinear D/A converter based on iterations is employed in the feedback path of the A/D converter. The synthesis of the nonlinear D/A converter is as follows: A difference equation for the given nonlinear function is first written and accordingly the circuit blocks, to be described later in this section, are connected to realize the function. A linear difference equation of nth order is given below and the

block schematic of the circuit to represent this equation is shown in Fig. 10. The equation is of the form,

$$V(D+n) + b_n V\ (D+n-1) + \ldots + b_1 V(D) = X(D+n) \tag{11}$$

where D, V and X represent digital input, output voltage and input to the system respectively.

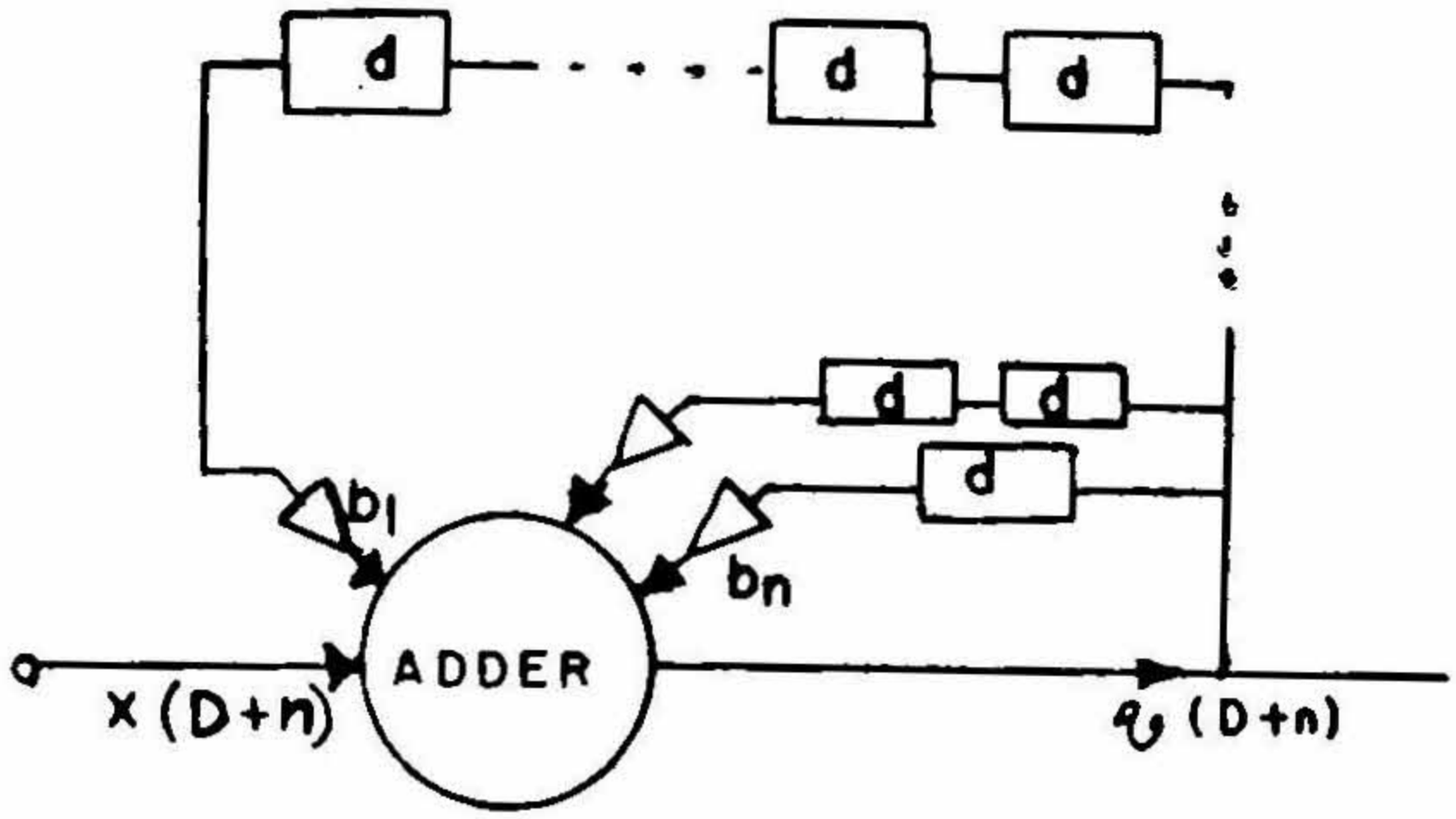

FIG. 10. Realization of difference equation.

The circuit of Fig. 10 consists of an adder, several controlled analogue delay units and amplifiers with gains ($b_1 - b_n$). As shown, the output $V(D+n)$ is fed back to the adder and the process is iterated. At the end of each iteration, the delay unit passes its input to the output. At the end of n iterations, Eqn. (11) is satisfied. In the case of D/A converters, the number of iterations is proportional to digital input D. Hence, a circuit to generate a burst of clock pulses, with the number of clock pulses being proportional to D is used in the D/A converter. The important constituents of this converter are (i) digital information to pulse burst converter, (ii) adder circuit, and (iii) analogue delay circuits, which are being described below. The block schematic of digital-to-pulse burst generator is shown in Fig. 11 (*a*). It consists of a digital comparator, a counter and a gated clock. The n-bit digital input and the output of n-bit counter are fed to the digital comparator, whose output is gated with the clock and the gate output is connected as input to the counter.

Initially the counter is reset and the comparator output is in '1' state, allowing the clock pulses to pass through the gate. The clock pulses are counted by the counter and this process continues till the counter output equals the digital input. At this stage, the comparator output changes to 'O' state thereby inhibiting the clock pulses from reaching the counter. Thus, a burst of pulses is obtained at the output terminal. It is easy to see that the number of pulses in this burst is proportional to the digital input. The number, N, is given by,

$$N = \sum_{i=1}^{n} a_i\ 2^n/2^i \tag{12}$$

where, $a_1 - a_n$ represent the digital data.

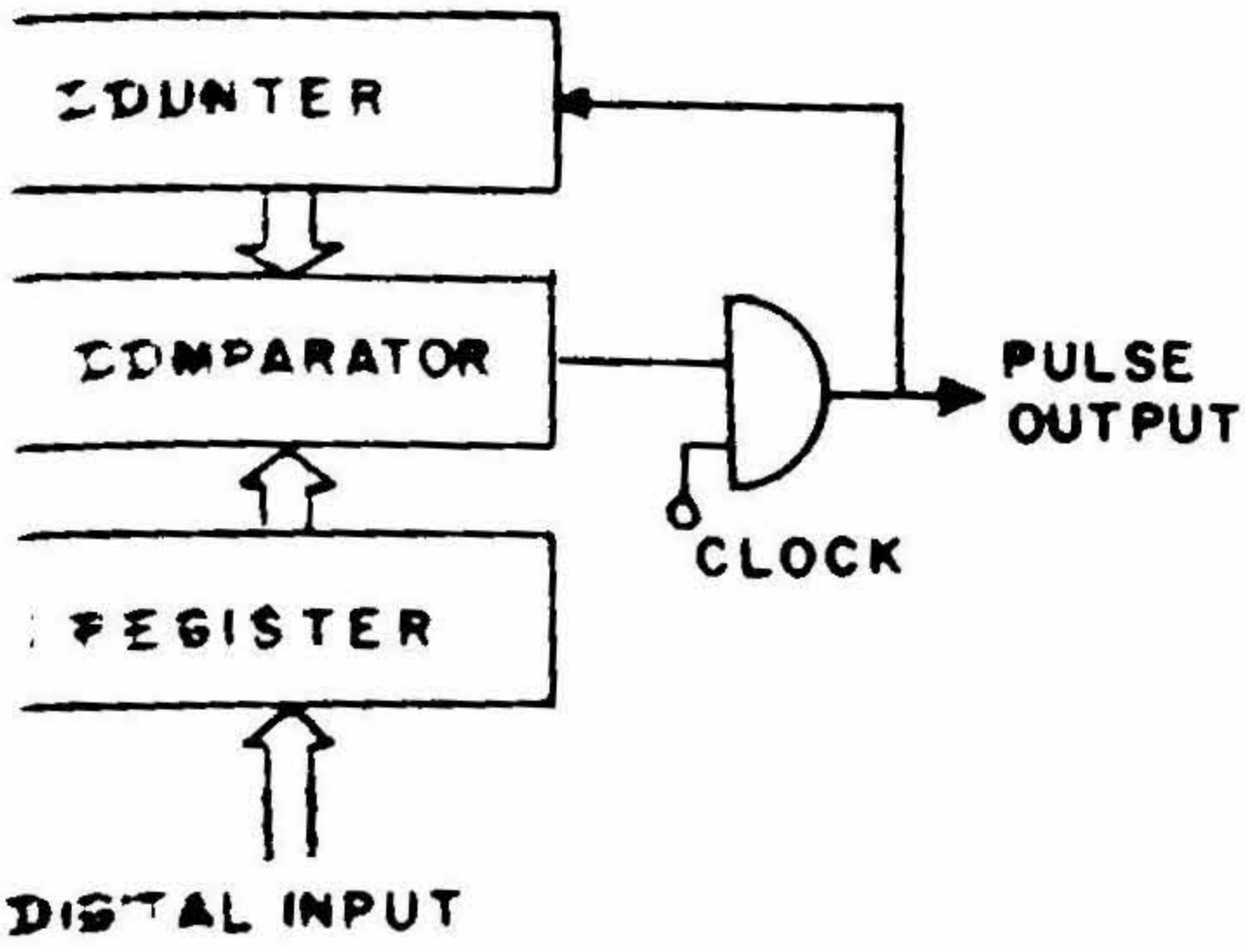

FIG. 11 (a). Digital-to-pulse burst converter.

The adder circuit is basically a summing amplifier employing an OPAMP. The OPAMP to be used is a high gain, high slew rate, high input impedance amplifier for good results. Fig. 11 (b) shows the schematic of an analogue delay circuit. It consists of two sample and hold amplifiers connected in cascade. Each sample and hold amplifier consists of a switch S, a capacitor C and high input impedance voltage follower. When the control signal, e, is in '1' state the switch S_1 is closed and C_1 charges to input voltage V_{in}. When e goes to 'O' state, S_1 is turned off and S_2 is turned *ON*, transferring the voltage held by C_1 to C_2 and the input voltage appears at the output. Thus, the input voltage is delayed by a time period determined by the control signal e. If the output from the pulse burst generator acts as the control signal, then the input voltage is delayed by one clock pulse, *i.e.*, the input appears at the output at the end of the clock pulse.

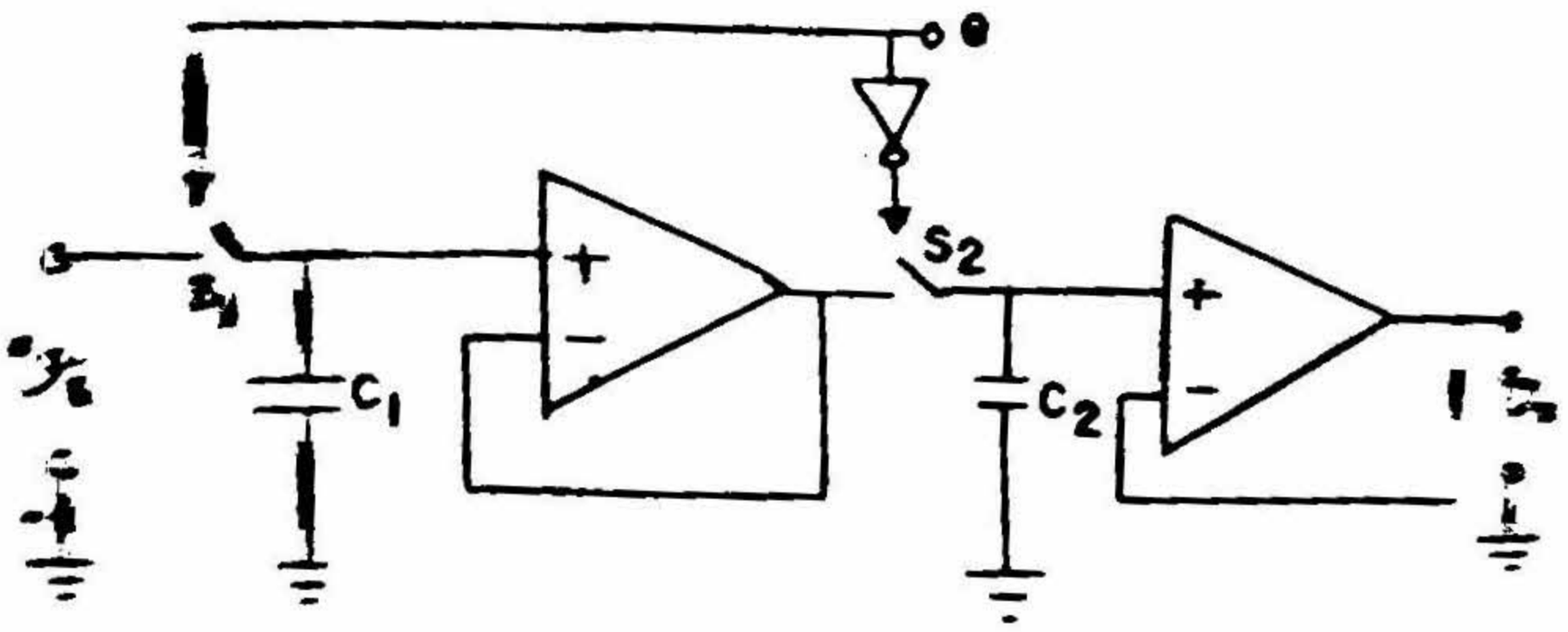

FIG. 11 (b). Analogue delay circuit.

In a similar way the input can be delayed by n-pulses by cascading n-delay units as shown in Fig. 11 (c). with the delay units being driven by clock pulses. At the end of the first clock pulse. the input appears at the first delay unit. In general, the input is transferred to the output of ith delay unit at the end of ith clock pulse.

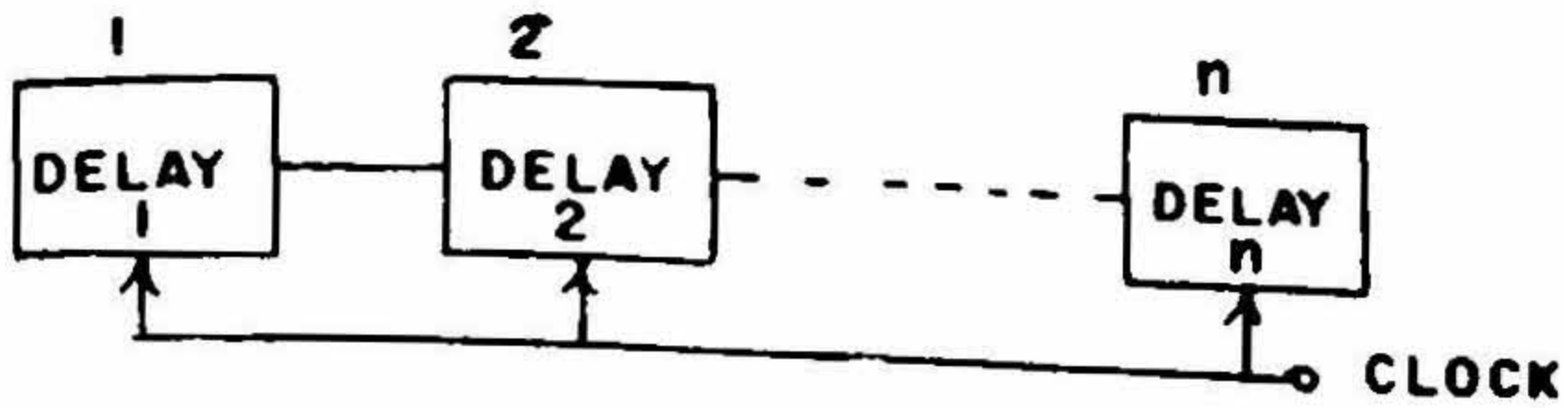

FIG. 11 (*c*). Delay unit.

FIG. 11 (*a*) to (*c*). Important building blocks of nonlinear D/A converter.

These units are connected as shown in Fig. 10 to realise the nonlinear D/A converter. With this method, different nonlinear functions can be easily generated by connecting the above constituents in an appropriate manner, determined by the relevant difference equation. Though the hardware complexity of this technique is low, the conversion time is quite high. The conversion time period varies with the digital input and the maximum time for an n-bit conversion is

$$t\,\text{con. (max)} = 2^n.\ t_c, \tag{13}$$

where, t_c is the time period of the clock pulses employed in the pulse burst generator.

The D/A converter described above can be used as a feedback block in nonlinear A/D converters. Since the conversion time period of D/A converter is large, only counter-ramp type converters can be realized employing this technique.

(c) *Conversion based on cascade connection of linear D/A converters*

Two generalized algorithms to implement nonlinear A/D converters are presented in the previous sections. In this section, a technique is explained which can generate a polynomial function utilizing linear multiplying D/A converters.

Fig. 12 shows the block schematic of an nth order polynomial D/A converter. It consists of n linear D/A converters connected in cascade and an adder circuit to sum up the outputs of all these converters. Each linear D/A converter consists of a register to store the digital data, a reference voltage source, switches, a resistance network (*eg.*, R-$2R$) and an OPAMP at the output terminals. It is clear from Fig. 12 that the output of ith D/A converter acts as reference voltage for $(i+1)$th converter and the digital input D is simultaneously applied to all the D/A converters. Therefore, the output of first D/A converter is given by

$$v_{01} = K_1 D \tag{14}$$

where K_1 is a constant. Since v_{01} acts as reference voltage for the second converter, its output v_{02} is related to D as follows :

$$\begin{aligned} v_{02} &= K\ .\ V_{01}\ .\ D \\ &= K_2\ .\ D^2 \end{aligned} \tag{15}$$

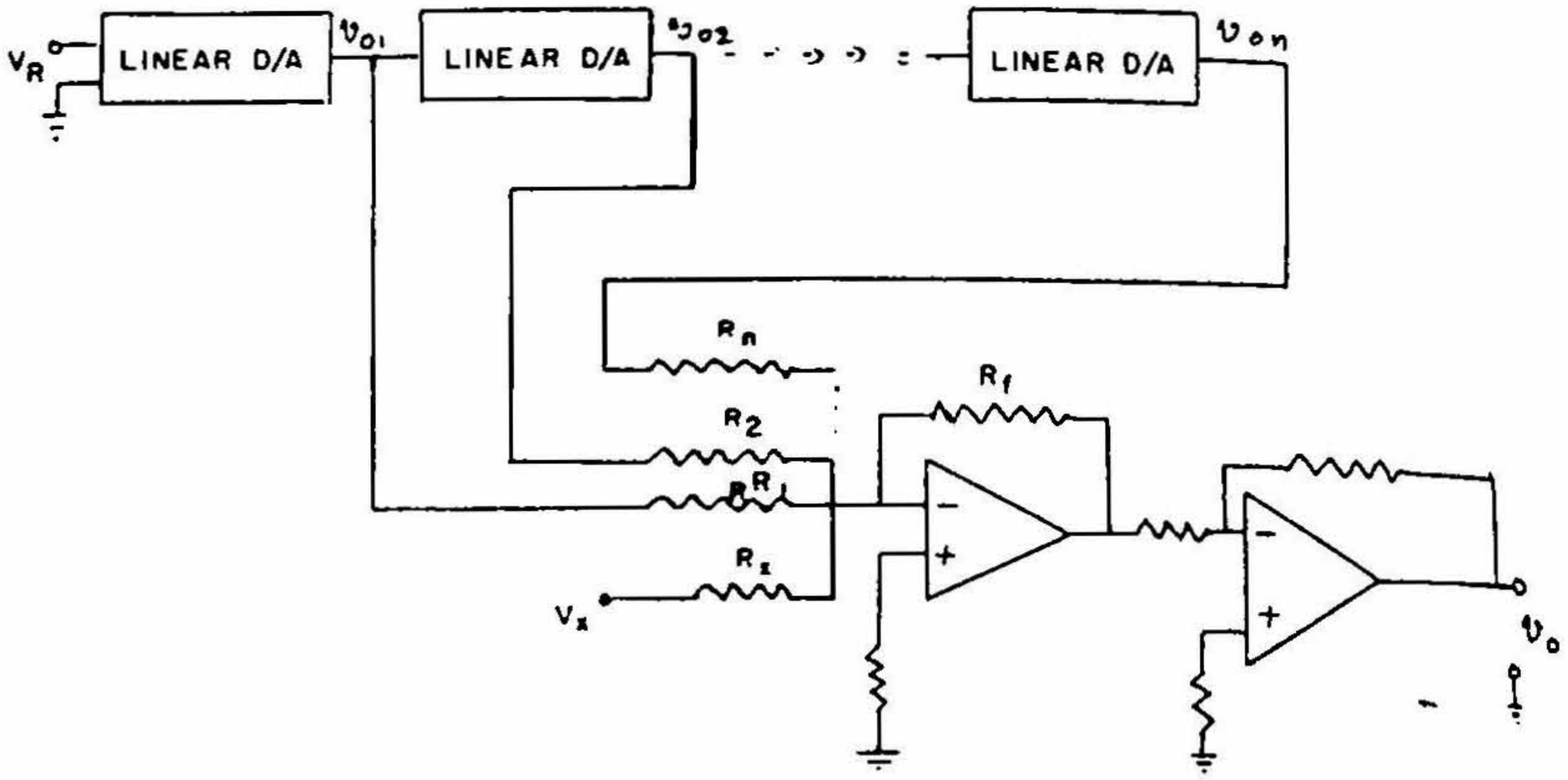

FIG. 12. Polynomial D/A converter.

In general, the output of ith D/A converter is given by,

$$v_{0i} = K_i \,.\, D^i \tag{16}$$

The output of the adder circuit is given by

$$v_0 = v_X/R_X + \sum_{i=1}^{n} (V_R \,.\, D^i/R_i)\, R_f \tag{17}$$

where, v_X is a fixed voltage as shown in Fig. 12. The above equation can be rewritten as,

$$v_0 = \sum_{i=0}^{n} b_i \,.\, D^i \tag{18}$$

where b_i is a constant. This constant is dependent upon the number of bits, m, in the digital input, the reference voltage V_R, the resistors R_i and R_f of the adder circuit. Evidently v_0 represents the nth order polynomial of D.

The polynomial D/A converter with a few modifications can be used to generate other functions also. Any function $f(D)$ can be expressed in terms of Maclaurin series as follows:

$$f(D) = f(0) + D.f'(0)/1\,! + D^2 \,.\, f^2(0)/2\,! + \ldots + D^n \,.\, f^n\,(0)/n\,! + \ldots \tag{19}$$

where, $f^n(0)$ represents nth derivative of the function at $D = 0$. A fairly accurate function can be synthesized even while using a limited number of terms of Eq. (19).

The main advantage of this type of D/A converter is that with only linear D/A converters and an adder circuit, several nonlinear functions can be generated to good approximation. The conversion period of the D/A converter is the sum of all the individual delays of each linear D/A converter. Hence the conversion period of the non-linear D/A converter is approximately 1 μ sec. The above nonlinear D/A converter is used to realize a polynomial A/D converter. Since the conversion period of this D/A converter is relatively small, high speed techniques like successive approximation can be associated with this for nonlinear quantization.

4. Experimental work

It is easy to implement the generalized techniques described in the above section. To demonstrate the effectiveness of these techniques, logarithmic and polynomial A/D converters were implemented. These are described in the following sub-sections.

(*a*) *Logarithmic A/D converter*

For a logarithmic A/D converter, it is necessary to have an exponential D/A converter. A D/A converter based on Haar functions is employed here. The block schematic of a 5-bit converter following this is shown in Fig. 13 (*a*). Initially the comparator input is high thereby enabling the clock pulses to reach the counter. The counter output drives the D/A converter. When v_0 equals v_i the output of comparator goes low, thereby inhibiting the clock pulses from reaching the counter. The output of the counter is therefore a logarithmic function of v_i. The input range is 0–5V and the maximum conversion period is 32 μ sec, when the clock frequency is 1 MHz. The transfer characteristic of the D/A converter is shown in Fig. 13 (*b*).

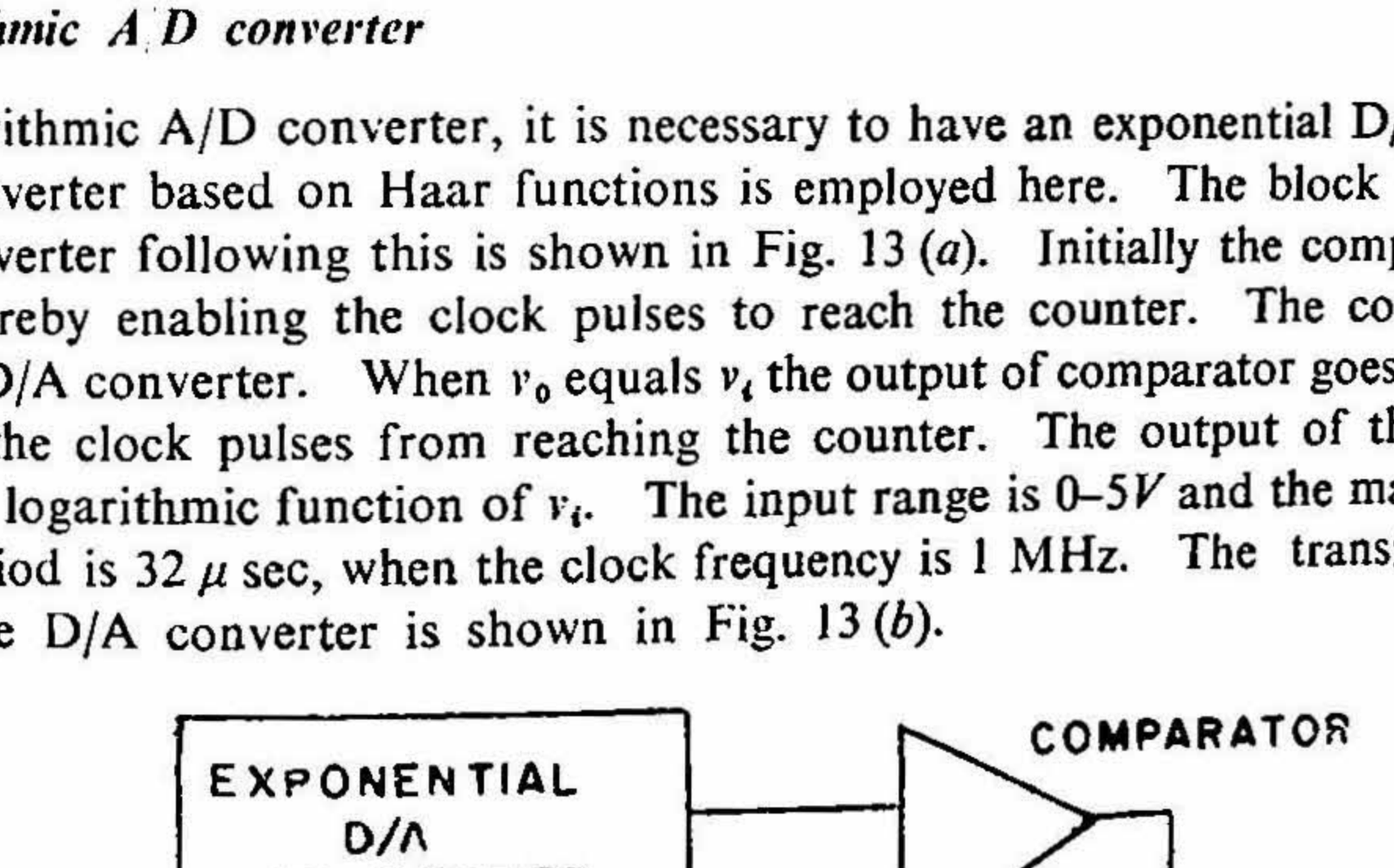

FIG. 13 (*a*). 5-Bit logarithmic A/D converter.

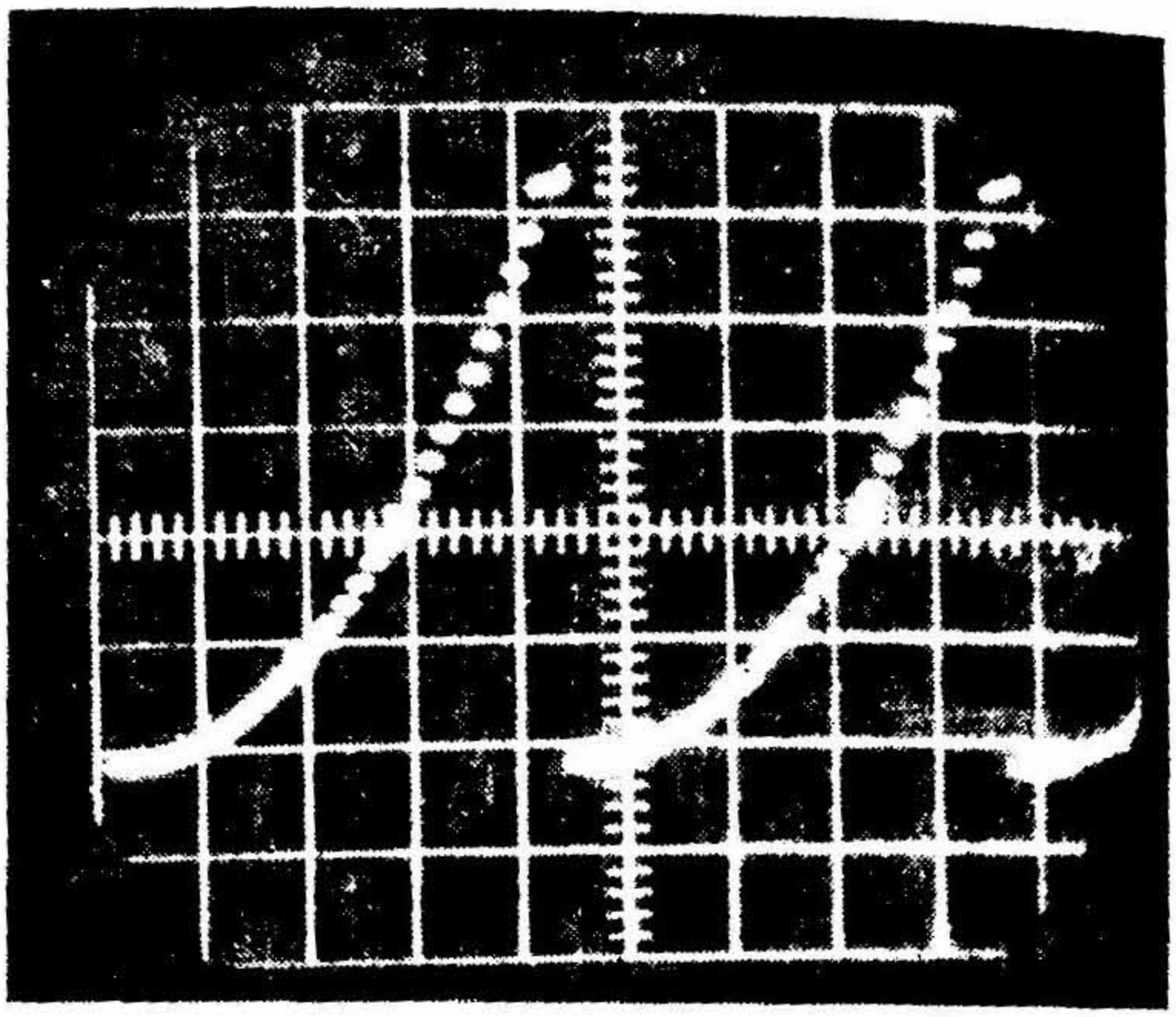

FIG. 13 (*b*). Transfer characteristic of exponential D/A converter. X-axis—10 μ sec/Div; Y-axis—1V/Div.

(*b*) *Polynomial converter*

The block schematic of a 2nd order A/D converter is shown in Fig. 14 (*a*). The D/A converter employed here is of the polynomial type and is described in sub-section 3 (*c*). The operation of the converter is similar to the counter-ramp type converter described in the above sub-section. When the quantization is complete the digital output is related to input voltage as follows:

$$D = av_i + bv_i^2 \tag{20}$$

where a and b are constants. The input voltage range is 0–5V and the maximum conversion interval is 32 μ sec when the clock frequency is 1 MHz. This converter is useful

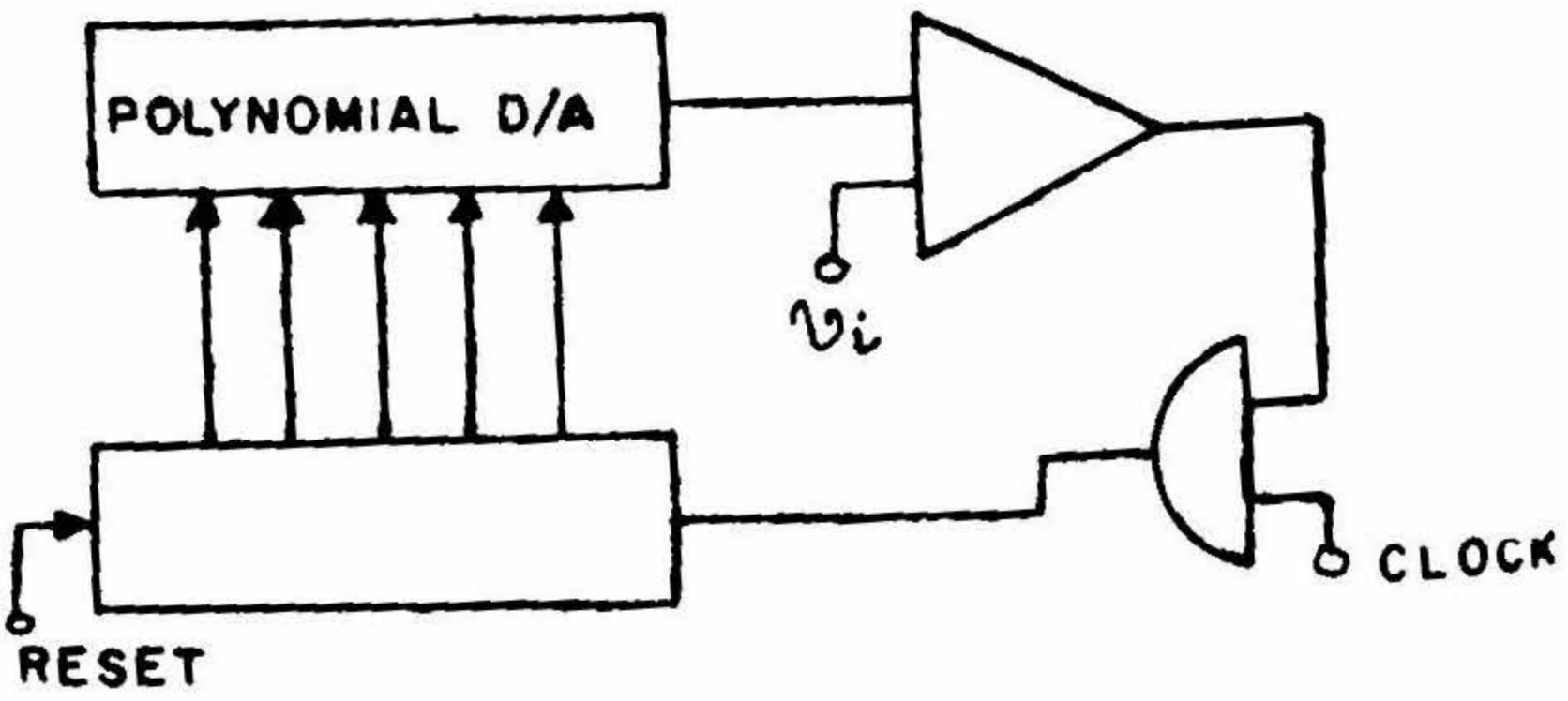

FIG. 14 (*a*). 5-Bit polynomial A/D converter.

in linearizing the outputs of certain nonlinear transducers like thermocouples. The transfer characteristic of the D/A converter is shown in Fig. 14 (*b*).

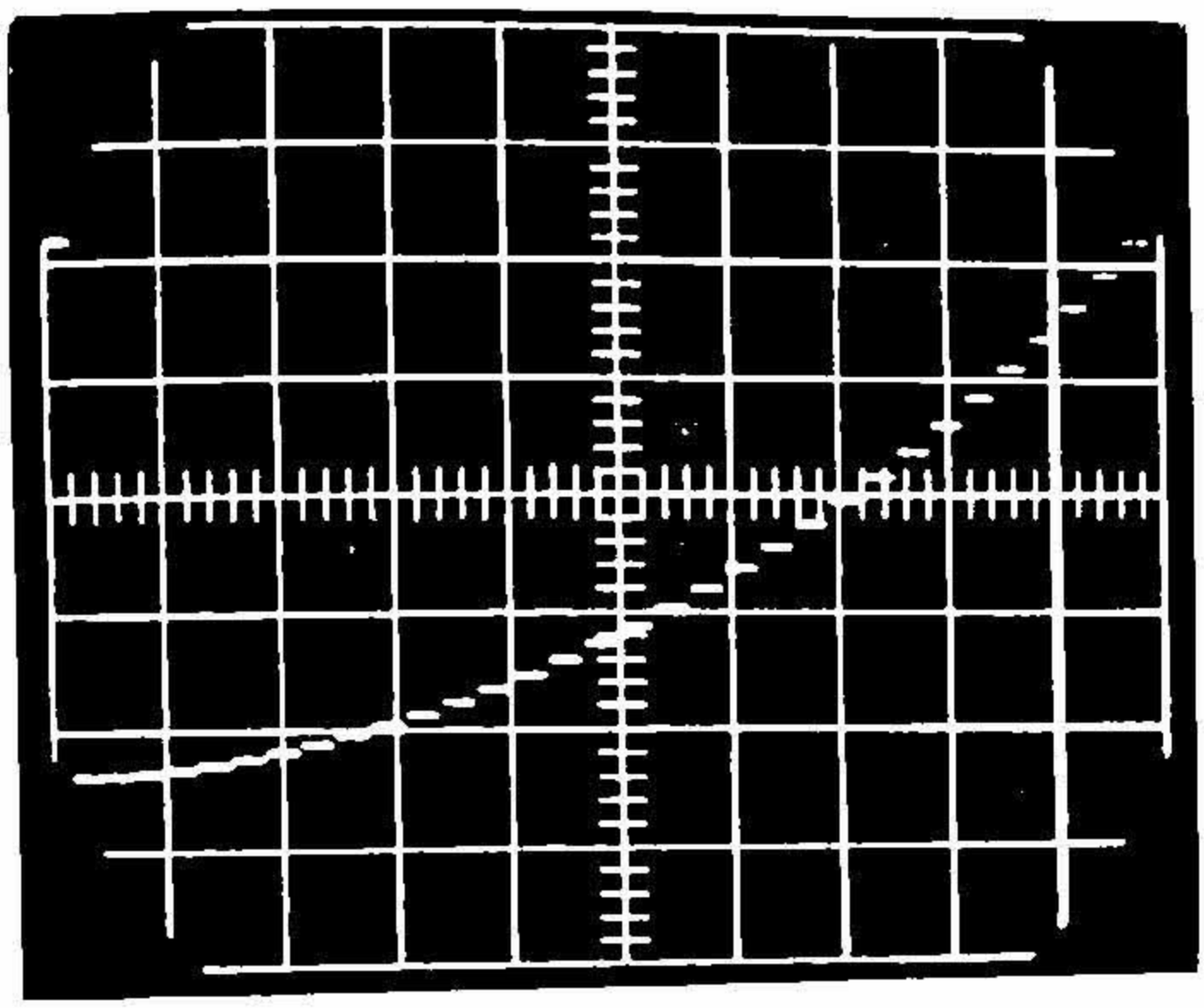

FIG. 14 (*b*). Transfer characteristic of polynomial D/A converter. X-axis—10 μ sec/Div; Y-axis—IV/Div.

5. Conclusion

The theory and practical implementation of nonlinear A/D converters using generalized algorithms are presented in this paper. The main advantage of the different techniques developed is their suitability for realizing a wide range of nonlinear characteristics with very few modifications in the hardware. Hence these converters are useful for a variety of applications in electronic systems.

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