Amorphous Hydrogenated Silicon: A Perspective on Circuit Synthesis

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Abstract | Non-crystalline or glassy semiconductors are of great research interest for the fabrication of large area electronic systems such as displays and image sensors. Good uniformity over large areas, low temperature fabrication and the promise of low cost electronics on large area mechanically flexible and rigid substrates are some attractive features of these technologies. The article focusses on amorphous hydrogenated silicon thin film transistors, and reviews the problems, solutions and applications of these devices.

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MOSFET: Metal-Oxide-Semiconductor Field Effect Transistors are electronic devices that are widely used as switches in modern day electronics. The switch turns on and off by the creation and destruction of a channel of charge carriers using field effect.

Large area electronics: Microelectronic circuits fabricated on substrates that have large surface areas—eg. display screens, image sensor arrays etc.

1. Introduction

Integrated circuit design in the 1990s was primarily focused on crystalline silicon MOSFET technology. Low power, and high speed operation with device scaling towards sub micron channel lengths were the highlights of research in semiconductor circuits. Around the same time there was another dimension to semiconductor engineering that was gaining momentum and was termed *large area electronics*.[1] Consider the flat panel computer display for instance—it is about 15 inches by 10 inches and typically has a liquid crystal to modulate the backlight. The liquid crystals are arranged in arrays of pixels, with a MOSFET switch addressing each pixel. How do we fabricate transistors across a 15 inch by 10 inch substrate? Conventional crystalline silicon wafer based fabrication would be a very expensive proposition. The answer is sought in an old technology where semiconductor materials are deposited as films over large substrate at relatively low temperature. Silicon for example is deposited using chemical vapor deposition by breaking down Silane at temperatures ranging from 140C to 450C. The low temperature deposition of semiconductors implies that the molecules of the semiconductor do not have sufficient time or energy to settle in the least energy position. This results in a loss of crystallinity resulting in films with no long range order.[2]

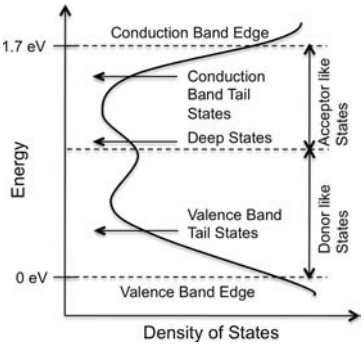
Low temperature deposition enables the use of substrates such as glass or plastic thereby promising electronics on materials that are mechanically flexible. This promise opens the door to many innovations—television sets that can be folded (Figure 1)[3], x-ray image sensors that can be conformably wrapped around the object to be x-rayed,[4] photovoltaic cells on large sheets, manufacturing of electronics using roll-to-roll processes[5] etc. These possibilities have brought a host of researchers from all disciplines to study materials, fabrication methods, modeling and system design. Figure 1 shows a mechanically flexible display demonstrated by Sony Corporation.[3]

On the materials front most of the research has focused on amorphous inorganics and organic crystalline and polymer semiconductors. Popular inorganic materials include amorphous hydrogenated Silicon (a-Si:H),[5] poly crystalline Silicon, and metal oxides such as amorphous Zinc oxide, Gallium Indium Zinc oxides, etc. Organics materials include small molecules such as Rubrene and Pentacene, and polymer semiconductors like Poly[5,5'-bis (3-dodecyl-2-thienyl)-2,2'-bithiophene] (PQT12), poly(3-hexylthiophene) (P3HT) etc.[6]

Fermi Level: The Fermi Level of a semiconductor is the energy level where the probability of finding an electron is exactly one-half. At 0K, the probability of finding electrons below the Fermi level is unity and the probability of finding electrons above the Fermi level is zero.

Figure 1: Demonstration of a mechanical flexible display. Courtesy—Sony Corporation.[3]

Figure 2: Illustration of Density of States in a-Si:H.



a-Si:H, however, has been the workhorse material in some sense and has been a material vastly studied. It is responsible for a lot of what we understand about disordered materials. This paper reviews the applications of a-Si:H in large area electronic systems, the problems of working with a-Si:H based TFTs from a circuit designers perspective and strategies to overcome these problems.

2. Density of States and Charge Transport

2.1. *Density of States*

The low temperature deposition of semiconductors implies that the molecules of the semiconductor do not have sufficient time or energy to settle in the least energy position. The resulting amorphous/glassy film therefore does not have long range order, and contains numerous defects such as broken bonds, stretched bonds and variations in bond angles. The absence of long-range order in a-Si:H leads to the presence of states in the band gap of the material as shown in Figure 2.[8] The presence of states in the band-gap has significant consequences.

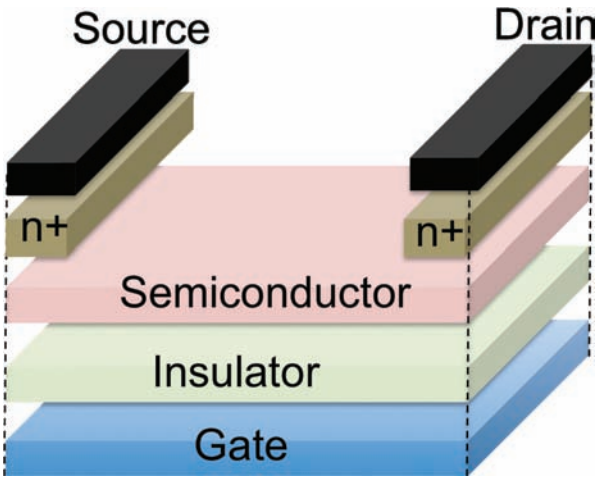
In the case of crystalline Si, we have a clear band gap separating the conduction and valence bands. However, in the case of a-Si:H, the presence of states in the band gap results in a cruder definition of the conduction and valence band.

The states in the band gap of a-Si:H that lie above the intrinsic Fermi level are called *acceptor like states* that are charged when filled and neutral when empty. On the other hand the states below the Fermi level are the *donor like states* that are neutral when filled and charged when empty. In the case of a-Si:H, there are more donor like states than acceptor like states and therefore the equilibrium Fermi level lies above the midgap. This has significant consequences from the point of view of circuit design. Since it takes less charge to pull the Fermi level closer to the conduction band edge as compared to the valence band edge, an n-channel transistor is more feasible (has a higher on current) at low bias voltages as compared to a p-channel transistor.

The states in the gap can be further classified as *deep states* and *band tail states*. The states that lie around the intrinsic Fermi level at the middle of the gap are called deep states while the states nearer the conduction and valence band edges are called band tail states. The deep states are primarily due to the presence of broken or dangling bonds. Thus, the hydrogenation of amorphous Silicon reduces the deep state density. The band tail states are due to the presence of weak bonds in the a-Si:H structure. The density of states measurements in a-Si:H have shown that the band tail states in a-Si:H have an exponential distribution.

Carrier transport in a-Si:H was made clear by Mott[2] who got valuable clues from an important paper by Anderson.[9] Carrier transport mechanisms in a-Si:H can be broadly divided into transport in the deep states, band tail states and extended states. Just as in crystalline semiconductors, the thermal excitation of carriers from the Fermi level to above the conduction band edge boosts extended state transport. However, due to the presence of traps, the effective conductivity of carriers is low. Hopping is the main mechanism of transport for carriers in band tail and deep states. However, the hopping in band tail states is strongly dependent on temperature, while hopping of carriers in deep states has a weaker temperature dependence. If the deep state density is significant, deep state hopping could become a significant mode of carrier transport at low temperatures. However, the passivation of dangling bonds with hydrogen results in negligible deep state conduction in a-Si:H.

Figure 3: Illustration of TFT structure.



3. Thin Film Transistors

Large area electronic systems such as displays and image sensors require large area deposition of non-crystalline semiconductor films. The fundamental building block of these systems has been the field effect transistor based on non-crystalline semiconductors, also called *thin film transistors* (TFTs).[10]

3.1. *Fabrication*

A typical structure of the TFT consists of a stack of insulator and semiconductor deposited over a planar gate electrode as shown in Figure 2. The source and drain electrodes are then deposited over the semiconductor, with doping at the contacts and some overlap with the gate electrode to ensure low contact resistance.

While there exist several geometries and process flows for a-Si:H based TFTs, a typical process flow is as follows. A gate metal layer of 100 nm of Mo-Cr is first patterned on a substrate (usually glass or plastic). A stack of 200 nm Si-N, 150 nm a-Si:H is then deposited with 70 nm n+ doped a-Si:H at the source-drain contacts. While Si oxides form a good dielectric for crystalline Si based field effect transistors, Si nitride is the dielectric of choice in the case of a-Si:H due to its relatively defect free interface properties. The gate dielectric vias are then patterned and etched after which 200 nm of Mo-Cr is deposited and patterned for source- drain contacts. The electrodes and n+ a-Si:H are etched in unwanted regions, and a-Si:H semiconductor islands are finally patterned.

3.2. *Current-Voltage Characteristics*

The current voltage characteristics of the a-Si:H TFT is primarily dictated by trap assisted extended state transport.[6,11] When the gate voltage of the TFT is raised from flat band potential, the Fermi level in a-Si:H moves towards the conduction band edge. Initially the Fermi level resides in the deep states, and most of the induced charge goes into the acceptor like deep states with negligible charge present as free carriers. As the gate voltage is increased further, the Fermi level moves into the band tail states. This gate voltage is defined as the threshold voltage (VT) of the TFT. When the gate voltage is increased further, the Fermi level begins to edge towards the conduction bad edge, but is strongly pinned by the large density of states in the band tails. However, some of the induced charge begins to appear as free carriers due to the proximity of the Fermi level to the conduction band edge. The presence of these free carriers boosts the on current of the TFT.

The electrostatics of the device is defined by Poisson's equation

$$\frac{\partial^2 \phi}{\partial x^2} = \frac{1}{\varepsilon_s}\left(n_f + n_{bt} + n_d \right) \tag{1}$$

where ϕ is the potential, x the distance through the depth (from gate-insulator interface to the back end of the semiconductor), ε_s the permittivity of the semiconductor, n_f the free carriers per unit volume, n_{bt} the charge per unit volume trapped in the band-tail states, and n_d the charge per unit volume in the deep states. In sub-threshold operation, the Fermi level rests in the deep states and n_f, $n_{bt} << n_d$. On the other hand, in the above threshold regime, n_f, $n_d << n_{bt}$, in the case of a-Si:H. Defining a characteristic voltage of band tail states, V_{bt}, and the thermal voltage V_{th} we can write

$$\begin{aligned} n_f &= n_{f0} \exp(\phi / V_{th}) \\ n_{bt} &= n_{bt0} \exp(\phi / V_{bt}) \end{aligned} \tag{2}$$

where n_{f0}, n_{bt0} are the flat band free carrier and band tail charge concentration per unit volume. The high concentration band tails charge contributes very little to the on current since its effective mobility is the hopping mobility which is far less compared to the extended state mobility. Thus, for estimating the on current, it is sufficient to have the free carrier concentration, which is expressed as

$$n_f = \frac{n_{f0}}{n_{bt0}^{\alpha}} n_{bt}^{\alpha} \tag{3}$$

with $\alpha = V_{bt}/V_{th}$. The reason for expressing the free carrier concentration in terms of the charge concentration in the band tail states is that although the band tail states contribute negligibly to the on

current, they still dominate the electrostatics of the device. In the above threshold regime, if C_i is the dielectric capacitance per unit area of the TFT having a semiconductor of thickness t_0, we can say

$$C_i(V_{gs} - V_T - v_c) \approx qn_{bt}t_0 \tag{4}$$

where V_{gs} is the gate-source bias, V_T the threshold voltage, and v_c the channel potential. Using (4) in (3) and noting that the on current in the TFT with channel width W, and channel length L (y-direction) is given by,

$$I = \mu q W n_f t_0 \frac{dv_c}{dy} \tag{5}$$

we solve (5) by integrating along the channel length from the source to drain electrode to obtain

$$I = \mu_{eff} \frac{W}{(\alpha+1)L} C_i^{\alpha} \times \left[\left(V_{gs} - V_T \right)^{\alpha+1} - \left(V_{gs} - V_T - V_{ds} \right)^{\alpha+1} \right] \tag{6}$$

Here μ_{eff} can be verified to be the trap assisted effective mobility. Typical parameters for a-Si:H TFTs are an effective mobility of 1 cmsq/Vs, dielectric capacitance per unit area of 20–30nF/cmsq, and threshold voltages of about 2 –5V. Typically, $a \approx 0.9$, and the current voltage characteristics of the a-Si:H TFT are not dissimilar from the crystalline Si field effect transistor. Nevertheless, there are significant differences in the details of TFT operation. For instance, we do not see a depletion region formation as in the case of crystalline Si MOSFETs. Instead, we see band bending in the semiconductor due to the charging of defect states. The threshold voltage in crystalline Si MOSFETs is defined as the gate voltage when the carrier concentration of minority carriers at the interface equals the dopant density. These concepts are irrelevant to a-Si:H based TFTs. Yet, while the electrostatics of crystalline Si MOSFETs are different from a-Si:H TFTs, the current voltage characteristics are remarkably close to (6) which makes circuit design with the a-Si:H based transistors less alien.

3.3. *Active Matrix Large Area Electronic Systems*

The a-Si:H TFT is the building block for large area electronic systems.[1] Since a-Si:H TFTs have low on currents, they are mostly used for applications related to low bandwidth. An ideal application spectrum is the design of electronics for human interfaces, eg. displays and image sensors. The key role of the TFT in these systems is as an access transistor and in some cases as a signal modulation circuit. The typical architecture of large area electronic systems is shown in Figure 4.

The architecture consists of an array (n by m) of pixel circuits. Each pixel circuit has a TFT switch-capacitor circuit at the front which either directly or indirectly (through a modulation circuit) drives/receives data to/from an actuator/sensor. The gate of the access switch is driven by a gate driver circuit (eg. a shift register) housed outside the array and driving the gate lines labeled row *1-n*. The data signals are provided/received by a data driver/receiver circuit also housed outside the array through the data lines labeled col *1-m*. During operation, the *j*th row of the array is pulled high while all the other rows are kept at ground potential. This allows all the access TFTs along

Figure 4: Typical architecture of active matrix large area electronic sensors or actuators.

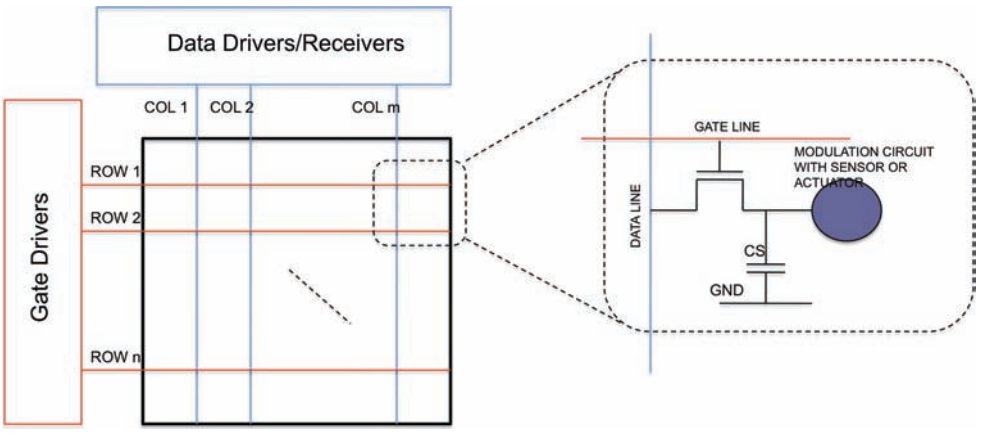
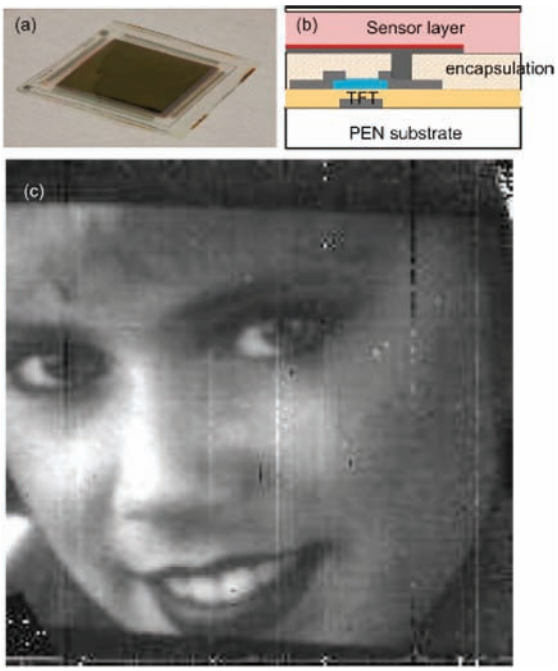


Figure 5: a-Si:H based image sensor array. (a) a-Si:H image sensor on plastic, (b) cross section illustration of the sensor circuit (c) the image sensed is read out and displayed.[12]



row *j* to remain closed while the other TFTs are open. Now, data from/to the sensor/actuator is received/sent by the data receivers/drivers via the data lines. Subsequently, the *j*th row is pulled to ground thereby opening the TFTs after which the (*j+1*)th row is pulled high. As this operation continues, all the pixels are scanned row by row at a desired frame rate. Figure 5 demonstrates an active matrix image sensor array fabricated on a flexible substrate using a-Si:H technology.[12]

4. Challenges in Circuit Design

4.1. *Threshold Voltage Shift*

The disordered nature of a-Si:H leads to the presence of states in the band gap of the semiconductor which is intrinsic to the semiconductor, as well as states at the semiconductor-insulator interface. The presence of these states leads to charge trapping during TFT operation thereby making the current-voltage characteristics a function of time.[13–21]

It was found that there are two primary mechanisms of charge trapping in a-Si:H TFTs.[13–21] The first of these mechanisms is charge *trapping at the interface*. When a gate voltage is applied to the TFT, carriers are drawn to the semiconductor-insulator interface where some of the carriers are trapped in shallow states. At high gate bias, carriers hop deeper into the insulator. High band gap, good quality dielectrics ensure that the latter is negligible during normal TFT operating bias conditions. The second mechanism is due to *defect state creation*. With applied gate voltage, the Fermi level moves into the band-tail states near the conduction band edge. The presence of carriers in the band-tails causes the weak bonds of the a-Si:H matrix to break. This results in new states being created deep in the band gap thereby lowering the Fermi level. Defect state creation is the dominant mechanism of carrier trapping at relatively low gate bias.

Both these mechanisms appear as an increase in the effective threshold voltage of the device with time. The threshold voltage shift (VT shift) in the a-Si:H TFT is therefore a function of the gate-source bias, drain-source bias and time. The gate and drain bias dependence of the VT shift is primarily due to the fact that the VT shift is proportional to the free carrier charge in the channel. The VT shift in a-Si:H TFTs is almost linearly dependent on the gate-source bias. The drain dependence of the channel charge determines the drain-source bias dependence of the VT shift. The time dependence of the VT shift is defined by the stretched exponential function. Thus the VT shift in a-Si:H TFTs can be compactly defined as[13–21]

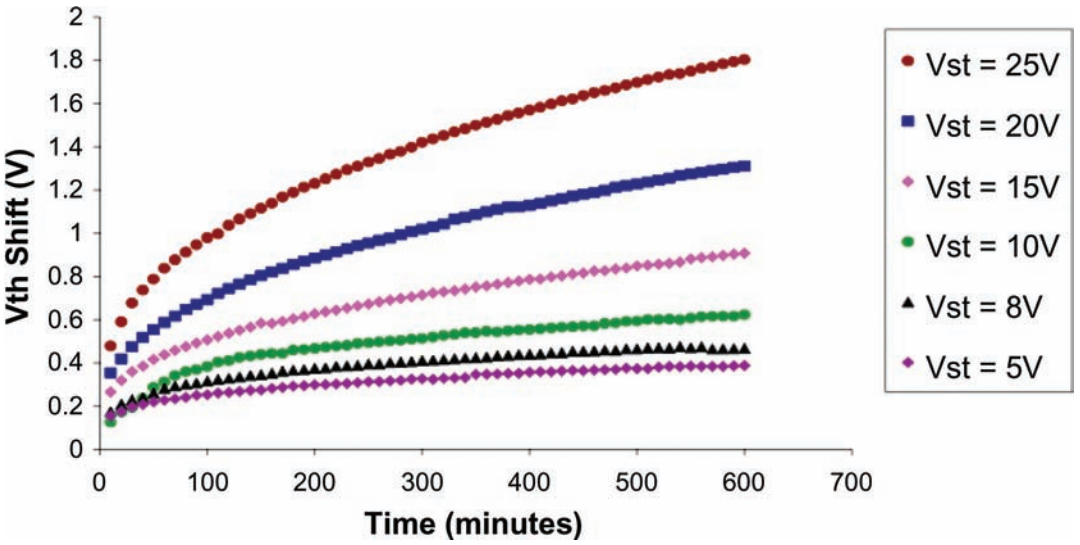
$$\begin{aligned} V_T(t) &= V_{T0} + \frac{2}{3} f_{Vgs} f_{Vds} \left(1 - \exp\left(-\left(t/\tau\right)^{\beta}\right)\right) \\ f_{Vgs} &= V_{gs} - V_{T0} \\ f_{Vds} &= \frac{1 - \left(1 - V_{ds} \Big/ \left(V_{gs} - V_{T0}\right)\right)^3}{1 - \left(1 - V_{ds} \Big/ \left(V_{gs} - V_{T0}\right)\right)^2} \end{aligned} \tag{7}$$

Here, V_{T0}, is the initial threshold voltage of the TFT, τ the characteristic time constant, and β a temperature dependent coefficient. When the TFT is in deep linear operation, $V_{ds} << V_{gs} - V_{T0}$, and $\lim_{V_{ds} \to 0} f_{Vds} = 3/2$. On the other hand, when the TFT just enters saturation, $V_{ds} = V_{gs} - V_{T0}$, and $f_{Vds} = 1$. Thus, the VT shift in the TFT in saturation operation is less than that in linear mode operation. Figure 6 shows the VT shift in the TFT in saturation and linear operation for various gate-source bias.

The VT shift in the TFT is partly recoverable. Since the charges are trapped in both shallow and deep states, reducing or reversing the gate-source bias quickly recovers the carriers trapped in the shallow states. However, charges trapped in the deep states are not so easily recovered and the device has to be annealed to bring the threshold voltage back to its initial values. The presence of

LED: Light emitting diodes are basically semiconductor junctions formed of two materials—one that has a predominant hole transport and the other that has mainly electron transport. When forward biased, the electrons and holes annihilate at the junction to emit light. In the case of inorganic crystalline semiconductors a p doped semiconductors and n-doped semiconductor are used to form the junction.

Figure 6: VT shift in an a-Si:H TFT for various gate (stress) biases.



this hysteresis in threshold voltage can be seen as an intrinsic memory within the device.

Consider the influence of the VT shift during device operation. When the TFT is used as a switch, the VT shift in time causes the TFTs on resistance to increase with time thereby causing errors in data storage. However, this is not a big concern since the increase in threshold voltage during the time when the switch is closed can be recovered/reduced when the switch is open. A more significant concern is during TFT operation as an analog device. Consider the display pixel circuit shown in Figure 7.

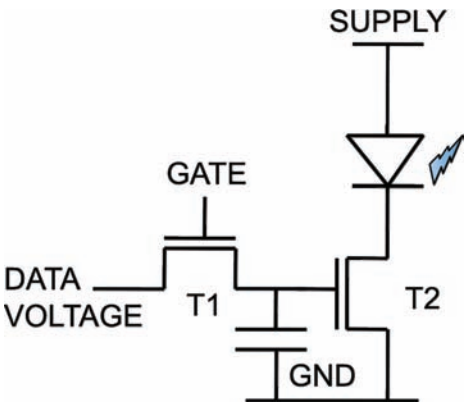
The pixel circuit drives a LED with TFT T2 behaving like a current source. First, the pixel access switch (TFT T1) is closed and the data to be displayed is stored on the storage capacitor, after which T1 is opened. Now the data that is present at the gate of TFT T2, programs T2 to sink a specific amount of current thereby controlling the brightness of the LED. Consider the influence of the VT shift on TFT T2. Since T2 gets a random sequence of data on its gate, the VT shift in T2 is unknown at any given point in time. Thus, the increasing VT in T2 causes the LED brightness to change in time for the same applied data voltage.

The influence of the VT shift in the TFTs makes the current-voltage characteristics a function of time. This is perhaps the most significant challenge faced by a circuit designer synthesizing circuits with non-crystalline semiconductor based TFTs.

4.2. *p-channel operation*

In the case of a-Si:H there are a larger number of donor like states as compared to acceptor like states.[11] Thus the equilibrium Fermi level lies slightly above the mid-gap. As the Fermi level moves towards the band edges, it is pinned by the large number of states in the band tails. Since there are fewer acceptor like states, a low positive gate bias is sufficient to induce free carriers in the conduction band. However, it takes a very large negative bias to push the Fermi level towards the valence band edge. This effectively implies that p-type TFTs are not practically feasible. The lack

Figure 7: Display pixel driver circuit.



of complementary TFTs is a major drawback of a-Si:H TFT technology.

5. Addressing the Challenges

The two main challenges discussed in the previous section are unique not only to a-Si:H TFTs but to non-crystalline semiconductors in general. While complementary devices were recently demonstrated in organic polymer semiconductors, the problem of the VT shift is even more severe in these materials. In this section, we study several circuit techniques that are useful tools for the circuit designer working with these materials.

5.1. *Threshold Voltage Shift*

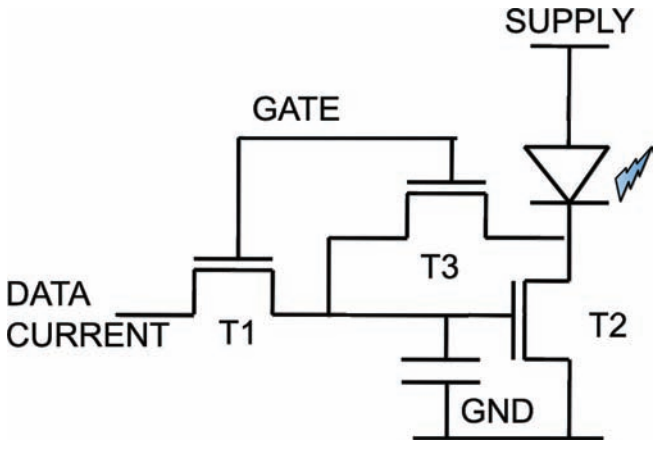
The VT shift in the a-Si:H TFT is attributed to charge trapping at the gate-insulator interface and defect state creation. It is dependent on bias conditions and increases with time as shown by the model described in (7). In the previous section, we saw the problems caused by the VT shift in the TFT highlighted by the LED pixel driver circuit of Figure 7. So how does one go about tackling the issue of the VT shift?

5.1.1. *Compensation Circuits*

If there is one critical TFT in which the problem of the VT shift creates problems for system operation, the best means of tackling the problem is by means of a compensation circuit.[22–23] The job of the compensation circuit is to estimate the threshold voltage in the critical device of interest and adjust bias conditions so as to compensate for the effect of the VT shift. Here, a key paradigm is that the compensation circuit must consist of only TFTs operating as switches as they do not need any compensation themselves. This is due to the fact that the VT shift can be recovered by applying a slightly negative gate bias. This can be done when the switch is turned off. Equivalently, the critical device is typically a TFT in analog operation.

As an example, we return to the circuit of Figure 7. Instead of programming the gate of T2 with a data voltage, we program the circuit of Figure 8 with a data current. Figure 8 shows a simple current programmed compensated pixel driver circuit. It includes a new TFT switch T3 that shares the same gate line as T1. During programming, both T1 and T3 are closed, and the data current now runs through the diode connected T2. Since there is a VT shift in T2, the gate of T2 sets itself to the compensated voltage required to ensure that T2 drives the data current. Once T1 and T3 are switched off, the gate of T2 has the correct compensated data voltage required to ensure that the same data current is sourced from the light emitting diode.

Figure 8: Compensation circuit with a display pixel circuit.



5.1.2. *Self Stabilization Circuit*

While compensation circuits are ideal when one TFT needs to be calibrated for its VT shift, they are not practical when all TFTs of a circuit are in analog operation. In such a case, a different strategy is required for circuit design.[24–25]

Here we ponder over the fact that unlike in the case of crystalline Silicon MOSFETs, the a-Si:H TFT by itself is not a fundamental building block. In other words, a building block for analog design must be reliable and not have time variant transfer characteristics. This is not true in the case of the a-Si:H TFT, where the drain-source current is a function of the VT shift in time.

While a general theory for identifying building blocks for non-crystalline semiconductor circuit design is provided elsewhere, an interesting effect of self stabilization was observed in certain types of TFT circuits. It was found that in circuits with symmetrical topologies, the transfer characteristic (plot of output vs. input) was not affected by the VT shift in the TFTs if it was dimensionless. In other words, the circuits had self-compensating behaviour if the input and output were of the same domain, either voltage (potential) or current (flow). This is a form of self-organization of functionality where it appears that one part of the circuit compensates for the VT shift in the other and vice versa.

Consider the common source voltage amplifier shown in Figure 9 with the aspect ratio of TFTs T1 and T2 being identical. Assume the gate voltages of T1 and T2 are V_B and V_I, respectively and that both TFTs are in saturation. At time zero, the output

CMOS: Complementary metal-oxide-semiconductor technology implies the use of both p-channel and n-channel MOSFETs.

Figure 9: Common source voltage amplifier.

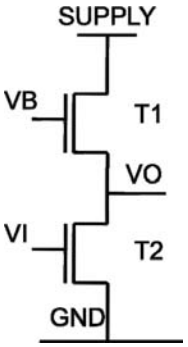
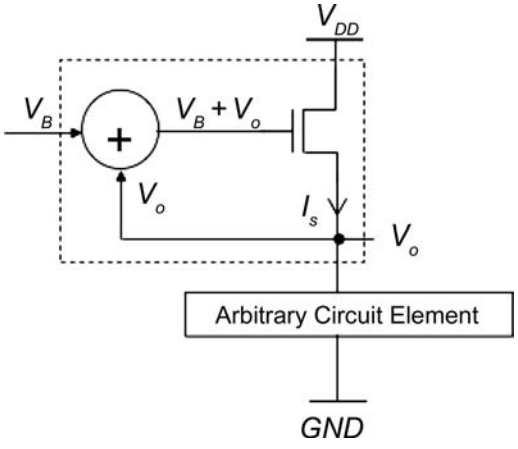


Figure 10: Concept behind the pseudo-PMOS.



voltage of the circuit is obtained by equating the currents in TFTs T1 and T2. If the mobility, and capacitance per unit area and threshold voltage in the TFTs are the same,

$$V_O(t=0) = V_B - V_I$$

Thus, according to (7) from the VT shifts in T1 and T2 are .

$$V_{T\_T1}(t) = V_{T0} + (V_I - V_{T0}) f(t)$$
$$V_{T\_T2}(t) = V_{T0} + (V_I - V_{T0}) f(t)$$

The output voltage at any given time is then again found by equating the currents in the two TFTs.

$$\left(V_B - V_O(t) - V_{T-T1}(t)\right)^2 = \left(V_I - V_{T\_T2}(t)\right)^2$$

This yields $V_O(t) = V_0(t=0)$. Thus, in spite of the VT shift in the TFTs, the output voltage remains time invariant. Note that the internal states of the system, in this case, the current, is time varying. However, the two TFTs adjust their respective impedances so as to keep the output voltage time invariant. More details and other classes of circuits are discussed elsewhere.[25]

5.2. *p-channel operation—A pseudo PMOS*

One of the important drawbacks with using a-Si:H technology was shown to be the lack of a p-type device. Using the common source amplifier as the starting point of our discussion, we understand the key reason for CMOS technology being desired. The dc gain of the amplifier Figure 9 with an n-channel load and driver is given by $-g_{mD} z_{out}$, where g_{mD} is the transconductance of the driver TFT and z_{out} is the effective load resistance. Since the driver and the load are both n-channel devices, it is seen that the effective load resistance neglecting channel length modulation is $1/g_{mL}$.

Therefore, the dc gain of the amplifier $-g_{mD}/g_{mL}$ can be improved only by the scaling of device geometries. On the other hand, if the load transistor is made a p-channel device, the output impedance goes ideally to infinite, since a p-channel device is a current source. In reality, the output impedance of the circuit would be limited by channel length modulation, which would still be high. The high gain achieved using CMOS devices is the reason for the success of digital electronics particularly in terms of negligible signal loss.

The important question here is – can we imitate a p-channel device using just n-channel TFTs. The answer to this question is in the affirmative if we use the concept of positive feedback.

In order to achieve a high output impedance, the current through the load TFT must not vary with voltage variation $V_O(t)$ in the output node. Thus, we need to feedback the output voltage of the amplifier to the gate of the load TFT, such that the gate receives a bias $V_F = V_B + V_O(t)$. The current through the load will then be determined by bias voltage V_B, which is held constant. This feedback is achieved by cascading two common source amplifiers as described elsewhere.[26]

6. Conclusions

Since non-crystalline materials are rather novel, research in the area of non-crystalline semiconductors has been predominantly oriented towards the materials and fabrication aspects. Novel materials such as carbon nanotubes, inorganic crystalline nanowires, graphene, organic

polymers etc are making their claim as being the material of choice for large area electronics.

This paper demonstrated that several problems such as those caused by the material and the device operation can be walked around using clever circuit techniques. Using a-Si:H technology as an example, we looked at the science of non-crystalline semiconductors particularly from the point of view of circuit design, systems and applications. While a-Si:H was used as an example of disordered semiconductors, the concepts discussed here are generally relevant to most disordered semiconductors.

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