Preface

The architecture of currently used computers was proposed by John Von Neumann in mid-1940s and is known as the *Von Neumann architecture*. In this architecture, a program to be executed is stored in a memory. A processing element (PE) retrieves one instruction of this program at a time, interprets it and executes it. At a time, the PE can execute only one instruction. The operation of the computer is *sequential*. The speed of such a sequential computer is limited by the speed at which a PE can retrieve data and instructions from the memory and the speed at which it can process the retrieved data. This speed is limited by the speed of electronic circuits used to build the memory and the processing element. The rate of increase of the speed of the fastest electronic circuits has been slow. For example, the arithmetic processor of Cray-1 supercomputer, built in 1978, took 12 nanoseconds to add two 64-bit floating point numbers, whereas Cray-YMP, built in 1988, took 6 nanoseconds. Further, the speed of electronic circuits is reaching their physical limit set by the speed of light. Thus it is not feasible to increase the speed of sequential computers which use a single PE beyond a limit. The only alternative for obtaining higher speeds is to use many processing elements to work in parallel. Such a computer which consists of a number of interconnected sequential computers which cooperatively execute a single program to solve a problem is called a *parallel computer*.

Many interesting questions arise in designing parallel computers. These are: How should sequential computers be interconnected? Should we connect a small number of very powerful computers or a large number of microcomputers? Are Von Neumann architecture computers the appropriate building blocks to build parallel computers? Should one formulate new programming languages to conveniently use parallel computers or are current languages adequate? How should tasks in a program be allocated to processing elements of a parallel computer to minimise execution time? Should one look for new problem-solving paradigms appropriate for use with parallel computers? How does one monitor and allocate resources in a parallel computer? How does one debug parallel programs? It is thus clear that parallel computing is a very fertile area for researchers.

Many research groups at the Indian Institute of Science are seriously working in this area and they are spread over many departments. The purpose of this issue is to present a sampling of the work done by various groups. It is however not possible to report here all the work that is done at the Institute. An annotated bibliography is presented which attempts to cover a large part of the work done by the Institute staff.

This issue has four papers received in response to a request from the Guest Editor and is representative of the work carried out at the Institute. The first paper entitled *Multidimensional multilink multicomputer* by Moona and Rajaraman presents the design considerations and the architectural features of a parallel computer built at the Institute.

This paper is followed by a paper by Mohan Kumar and Patnaik entitled *Performance studies of a transputer-based extended hypercube*. Transputer is a computing element specially designed as a building block of parallel computers. This paper describes how well such a computing element performs in a parallel system which interconnects them in an extended hypercube structure. The third paper *A parallelizing compiler for Pascal* by Dave and Srikant addresses the important topic of language design for parallel computers. This paper explains the considerations in the design and on implementation of a parallelizing Pascal compiler. The fourth one *A parallel fast convolver for computer vision* addresses an interesting application of parallel computers in computer vision. This paper by Ramani, Srikanta, Venkatesh and Raymond describes a fast convolver used in computer vision which works in parallel. The issue concludes with an annotated bibliography of papers published during the period 1985-1991 by various researchers at the Institute on parallel computers and their applications.

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Guest Editor