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Design and fabrication of quasi resonant converter

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Abstract

This paper presents the design and fabrication of a Quasi Resonant Zero Current Switched DC to DC converter operating in the Full Wave Mode. The focus is on the working principles i.e., design and hardware implementation of the converter. The converter configuration and its control, have been suitably modified to ensure reliable operation during transient conditions, without compensating on the switch current ratings. Relevant analysis, SPICE simulation results, design procedure, hardware details, and experimental verification have been included.

Introduction

The need for resonant switching in converters stems from the desirable advantages of high frequency operation viz., lower reactive component values, smaller size of magnetic components (giving a high power density), and reduced EMI, as compared to hard switched PWM converters. The trade-off is in the higher current or voltage ratings of the switches due to resonant peaks.

This paper presents the design and implementation of a Quasi Resonant converter which is meant to replace a Push Pull type hard switched converter currently used for ac drive applications. The principles of Quasi Resonant converters are well known[1,2,3,4]. However, to the authors' knowledge, there is no literature available on the implementation aspects of the full wave mode Zero Current Switched (ZCS) Boost converter.

The basics of Quasi Resonant converters, the choice of configuration for the application, and its steady state operation are explained in Section 2. The modification proposed is described in Section 3. Design and simulation results, hardware implementation, and experimental results are included in Sections 4, 5, and 6 respectively.

2. Quasi Resonant Converters (QRCs)

This section describes the concept of resonant switches, the choice of converter configuration based on the availability of switches, and the steady state operation of the ZCS full wave mode boost converter.

2.1. *Resonant Switches*[1]

Quasi resonant converters have the same topology as PWM converters with the switch modified to a *resonant* switch. The resonant switch has a resonant inductor, a resonant capacitor, and a diode connected to the actual switch. For zero current switching the inductor is connected in

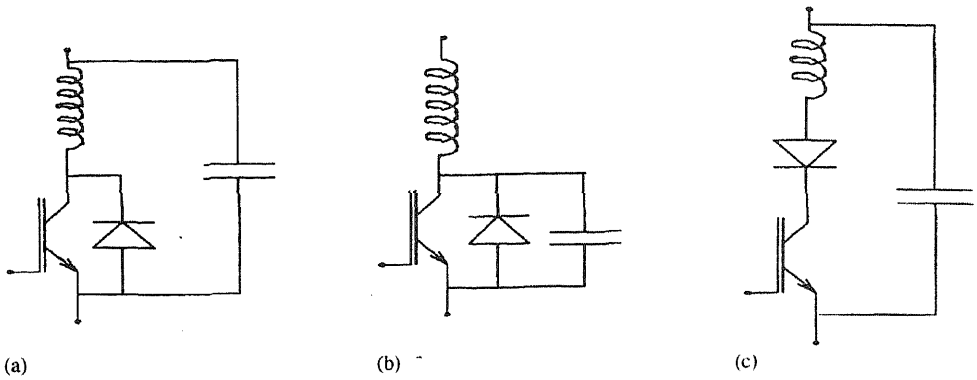


FIG. 1. Resonant switches (a) Zero Current Fill Wave Mode (b) Zero Voltage Half Wave Mode (c) Zero Current Half Wave Mode

series with the actual switch, and the capacitor is connected in parallel with the series combination [Fig. 1(a)]. Fig. 1(b) shows a zero voltage switch. For ZCS in the *Full Wave Mode* (and ZVS in *Half Wave Mode*) the current reverses through the resonant switch, so there is a diode connected in anti-parallel with the actual switch. For ZCS in *Half Wave Mode* (unidirectional switch conduction, and bidirectional voltage blocking) a diode is connected in series with the actual switch as shown in Fig. 1(c).

2.2. *Choice of Configuration*

Minority carrier devices leave a current tail at turn OFF when hard switched. The available switch, IGBT, being a minority carrier device, zero current switching is preferable. Also, Latch-up problems in IGBTs (due to parasitic thyristor) are alleviated with zero current switching, especially in the full wave mode. The full wave mode has the additional advantage of load insensitivity[1]. Therefore, a Zero Current Switched (ZCS) converter in the full wave mode [Fig. 2] was selected.

2.3. *Steady-State Circuit Operation of QR ZCS Full Wave Mode Converter*

It is assumed that, the boost inductor (L) is large enough, so that V_{DC} and L together may be regarded as a constant current source, the output voltage is constant, and the load is resistive.

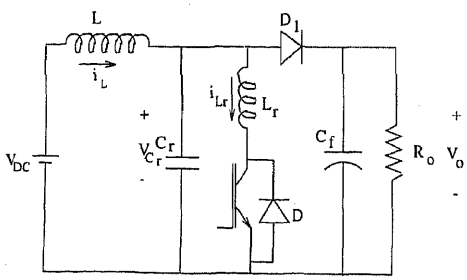


FIG. 2. QR Zero Current Switched Converter in Full Wave Mode.

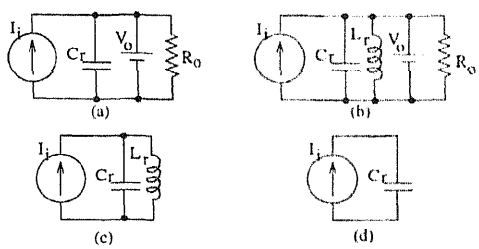


FIG. 3. Equivalent circuits: (a) Mode 1, (b) Mode 2, (c) Mode 3 and (d) Move 4.

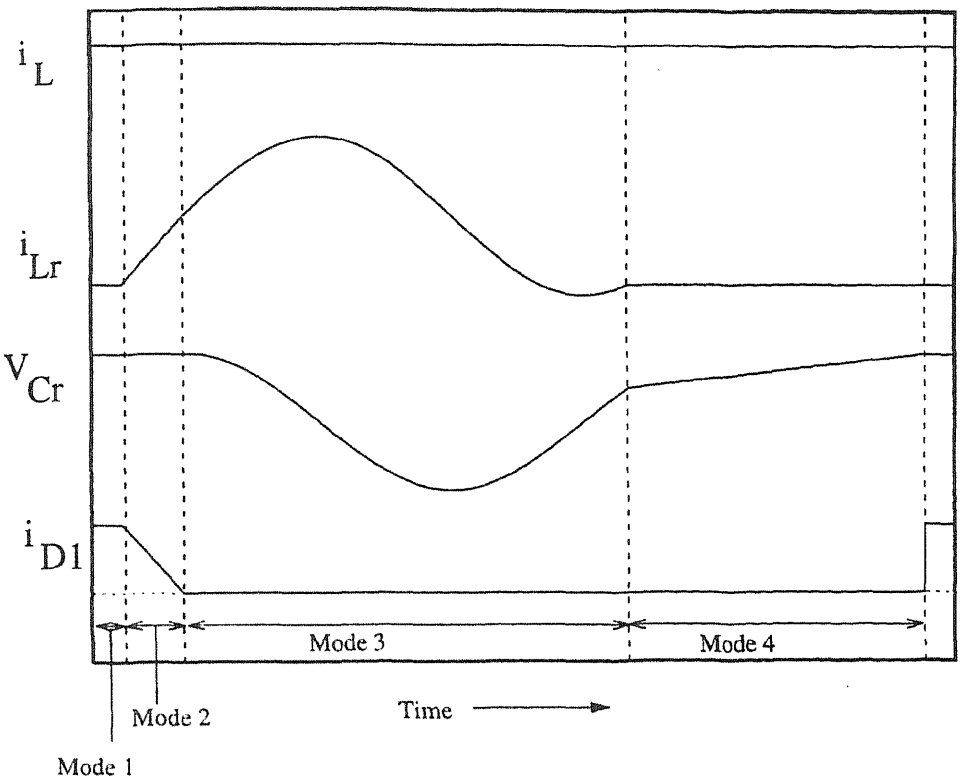


FIG. 4. Steady-State Operation: Voltage and Current Waveforms.

The circuit operation can be divided into different modes depending on the state of the switch and the diodes [Figs. 3, 4].

MODE 1

In this mode diode D1 is ON, and the switch is OFF. Therefore, the entire input current flows through D1.

MODE 2

This mode starts when the switch is turned ON. As long as D1 is ON, the resonant capacitor (C_r) voltage remains constant. So, the resonant inductor current (i_{Lr}) builds from zero and rises linearly till $i_{Lr} = i_L$, (and the current through the diode D1 decreases from i_L to zero). At this point the diode D1 turns OFF. Thus, the switch turn ON is at zero current. The diode turn OFF is at zero current, and the voltage across it builds up in a sinusoidal manner [Mode 3]. Therefore, a fast diode is not required.

MODE 3

After D1 turns OFF the circuit reduces to a parallel L-C combination with current source as input. The current through the resonant inductor (L_r) goes to zero, after which gate/base pulse to

the switch is removed. i_{Lr} reverses through the anti-parallel diode D. Hence the switch turn OFF is also at zero current. It is essential for i_{Lr} to reverse, so that the switch can be turned OFF. To satisfy this condition the peak resonant current $\left(= v_o\sqrt{\frac{C_r}{Lr}}\right)$ should be greater than the input current, I_i.

Assuming lossless converter,

$$I_i = I_o \times gain$$

$$V_o\sqrt{\frac{C_r}{L_r}} > \frac{V_o}{R_o} \times gain$$

$$\frac{R_o}{\sqrt{\frac{L_r}{C_r}}} > gain$$

$$\Rightarrow r > gain$$

Thus, the normalised load (r) has to be greater than the gain required. Also, the reversal of current through the anti-parallel diode has to be sensed following which the gate/base has to be disabled.

MODE 4

Since the switch is turned off i_{Lr} goes (from negative) to zero. In this mode the switch as well as both the diodes are OFF. The resonant capacitor charges linearly to V_o, following which the diode D1 turns ON, and the circuit operates in MODE 1.

The converter gain is controlled by the ratio of ON-time to the switching time period. The ON-time of the switch is decided by the resonant frequency and the load. The OFF-time can be controlled by the switching frequency, which therefore, controls the DC conversion ratio.

The gain of the converter, x, is given by[1] :

$$\left(\frac{x-1}{x}\right)-\left(\frac{1}{2\pi}\right)\left(\frac{f_{sw}}{fr}\right)\left[\left(\frac{x}{2r}\right)+\sin^{-1}\left(\frac{-x}{r}\right)+\left(\frac{r}{x}\right)\left\{1-\sqrt{1-\left(\frac{x}{r}\right)^2}\right\}\right]=0$$

where $1.5\pi < \sin^{-1}\left(\frac{-x}{r}\right) < 2\pi$

r the normalised load

f_{sw} switching frequency

f_r resonant frequency

3. Proposed Modification

The modification is necessitated by ringing at turn OFF, and transient operation of the circuit.

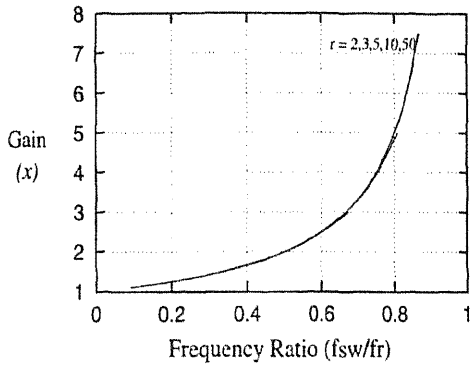


FIG. 5. DC voltage conversion ratio of quasi resonant boost converter in the full wave mode.

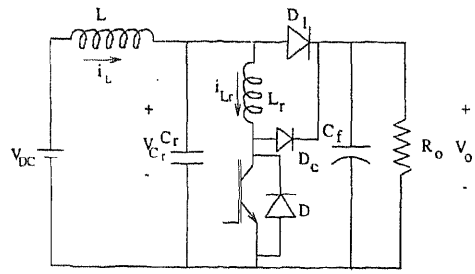


FIG. 6. Addition of the Diode Clamp.

3.1. *Switch Voltage Clamp*

When the resonant inductor current, i_{Lr} goes (from negative) to zero the collector to emitter capacitance of the IGBT has to charge through the inductor L_r resulting in ringing. This can cause the collector to emitter voltage to rise up to nearly twice the resonant capacitor voltage at that moment. This voltage peak will occur in each cycle. Thus, the voltage blocking capability of the switch may have to be increased.

To avoid this peak the switch voltage needs to be clamped. The collector to emitter voltage is limited to the output voltage by connecting a fast recovery diode from the collector of the switch to the output [Fig. 6]. This diode will be reverse biased as long as the collector voltage is less than the output voltage, which is the case throughout the entire operation, except during ringing at turn OFF.

3.2. *Transient Operation*

If the switching frequency is increased, to increase the output voltage, the immediate effect is a reduction in the conduction period of D1 [Fig. 6]. This causes the output voltage to decrease for some time while the boost inductor current, i_L, increases. Only after the inductor current has increased to a sufficient value does the output voltage start increasing again. The current i_{Lr} is the sum of i_L and the resonant current $\left(V_o\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t)\right)$ during Mode 3. Since V_o decreases while i_L is increasing, it is possible that the current i_{Lr} may not reverse. Due to this the converter will encounter problems during start up, and failure to turn off the switch (since current reversal is not sensed) will lead to short circuit of the input supply.

Normally, the switch should be turned OFF only when the current (i_{Lr}) reversal is detected (and before the current becomes positive again). However, in such a case the switch should be turned off after a prefixed maximum ON-time. The clamp diode, Dc, provides a path for the resonant inductor current i_{Lr}. This diode need not be of high current rating since i_{Lr} at the time of turn OFF will be close to zero. With the modification suggested the converter will start as a hard switched converter, although the switch current at turn OFF will be lower than the boost

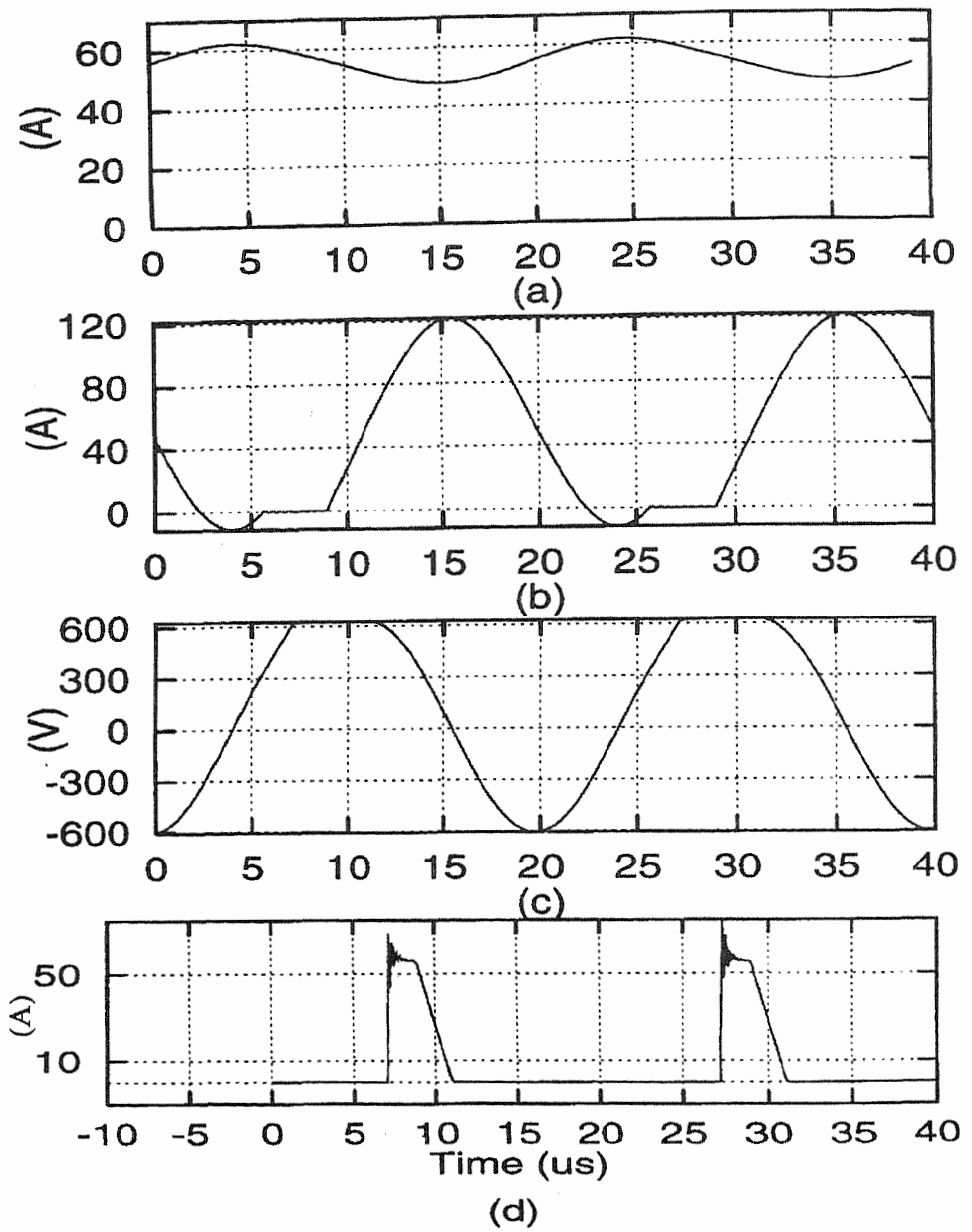


FIG. 7. Simulation Results: (a) Boost inductor current (i_L) (b) Resonant inductor current (i_{Lr}) (c) Resonant capacitor voltage (V_{cr}) (d) Rectifier diode current (i_{D1}).

inductor current (as is the case in the conventional PWM converter), and will automatically go into soft-switching once the output voltage rises.

One alternative solution is to increase the resonant current value, by decreasing the characteristic impedance, at the cost of increasing the peak switch current. Another possible way of avoiding the situation mentioned above is to make the control very slow, so that the frequency change is very gradual. This, however, will lead to problems in regulating the output voltage, and is therefore not practical.

4. Design and Simulation

The design is based on the already stated principles. The converter was designed for 5 kW, for an input of 90 V to 140 V (nominal voltage 110 V) DC, and a regulated output of 630 V DC.

Load resistance $R_o = \frac{630^2}{5\times10^3} = 79.83\ \Omega$.

Maximum Switching frequency was chosen equal to 50 kHz.

The boost inductor was chosen equal to 300 μH.

Using Fig. 5 a gain of seven can be achieved for a frequency ratio equal to 0.85 giving $f_r \approx 58.8$ kHz.

A constraint already mentioned is : $r > x$, the maximum gain. This defines the upper limit for the the characteristic impedance, $Z_n = \sqrt{\frac{L_r}{C_r}} < \frac{79.38}{7}$. The lower limit for Z_n is imposed by the peak switch current. If the Z_n is very low then the peak resonant current $\left(= \frac{V_o}{Z_n}\right)$ will be very high, thereby increasing the switch current rating. Keeping sufficient negative current (≈ 7 A) in the resonant inductor, which allows for sensing of current reversal, the values of C_r and L_r were calculated. Inclusion of parasitic resistances requires an increase in the frequency ratio. *SPICE* simulation was carried out and the specifications could be met for $L_r = 25.25\ \mu$H, $C_r = 0.33\ \mu$F, $r = 9.07$. The peak resonant current was found to be 72 A. The negative peak of i_{Lr} was 7.1 A, and the minimum conduction period of the anti-parallel diode (corresponding to minimum input voltage and maximum load current) was found to be 4 μs. Filter Capacitor $C_f = 15\ \mu$F was used in the simulation.

Component ratings were obtained from *SPICE* simulation of the converter. Waveforms obtained from the simulation are shown in Fig. 7. The implementation details of the converter are covered in the next section.

5. Hardware Implementation

The power stage consists of the basic converter as shown in Fig. 8. A fuse was added at the input to protect the input DC supply against short circuit. The diode D_F provides a path for the inductor current when the fuse *blows.*

Control Circuits

The converter has to be operated in closed loop with a PI controller, so that the output voltage follows the set value. A soft-start circuit is used to ramp the set value from zero (or previous

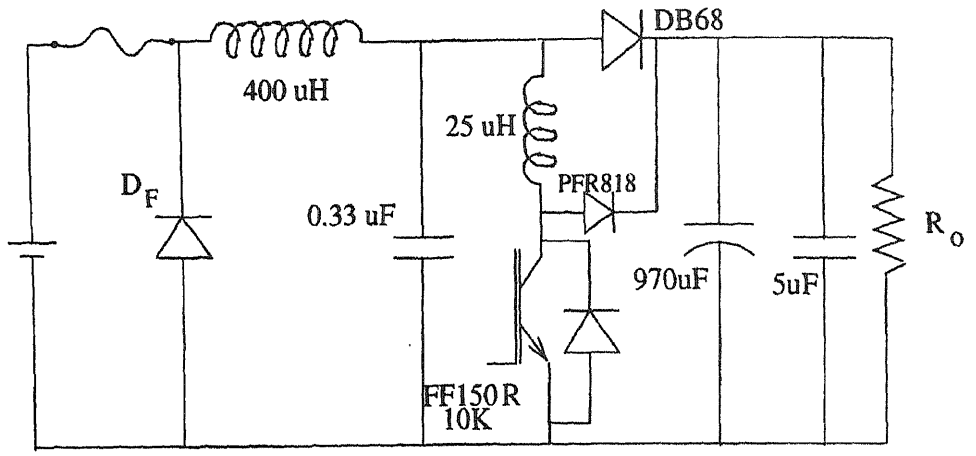


FIG. 8. Power Stage.

value) to the final value in a fixed time. The reference generated is given to the PI controller, which is followed by a limiter connected to a VCO.

5.1. *Gate Pulse Generation Circuit* [Fig. 9]

The gate pulse has to be maintained as long as the resonant inductor current, i_{L_r}, is positive, and should be removed as soon as its reversal through the anti-parallel diode is sensed. The inductor current reversal is sensed by detecting zero-voltage crossing of the switch voltage. The signal so obtained is clamped to a high value for 6 μs, so that ringing does not generate a faulty signal. To minimise delay, inherent in opto-couplers, this signal is coupled to the control circuit ground by means of pulse transformers. Pulses generated (using monoshots) at both the leading and the falling edges are transferred. The signal is reconstructed using a D-latch. It is ensured that there is a minimum delay of $\approx$ 800 ns between the positive and the negative edge pulse, so that there is no problem in reconstruction of the pulse by the D-latch. The signal, V_d, is the sensed switch (collector to emitter) voltage. V_d high implies that the switch is either conducting (and has a positive voltage drop), or the switch is OFF (and blocking a positive voltage). V_d low indicates that the anti-parallel diode is conducting. The switching frequency is controlled by the VCO. The VCO output is converted to pulses of 1 μs duration. If V_d is high and a pulse comes from the VCO, then, a high is latched at the output of the D-latch (positive edge triggered). When V_d goes low (i.e. the resonant inductor current reverses) data input is low, and a clock pulse is generated, thereby latching a low at the output.

The total available time, during which the current reversal has to be sensed and the gate voltage pulled to a low value, is 4 μs. If the current reversal is not sensed within 16.5 μs of turn ON, the monoshot M2 disables the gate signal and therefore limits the ON–time of the switch. In normal operation the transition of V_d from high to low generates a 1 μs pulse which resets the monoshot M2. The maximum ON–time was determined using the simulation results obtained for full load at minimum input voltage.

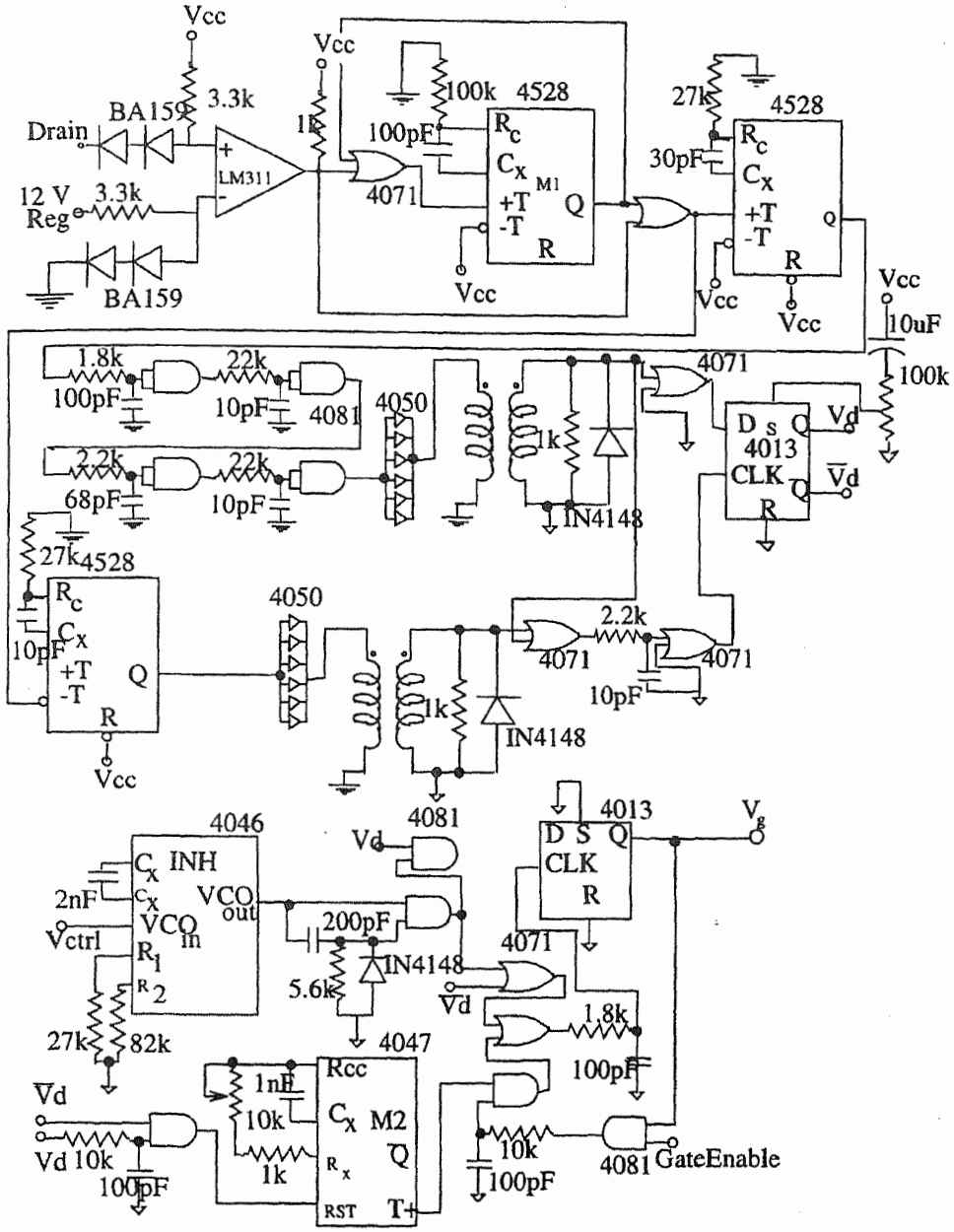


FIG. 9. Gale pulse generation circuit.

A hybrid driver module was used for isolation, and driving the IGBT [Fig. 10]. The total time required to pull the gate to a low voltage after the switch voltage (simulated) goes negative was observed to be 2.5 μs against the required maximum 4 μs.

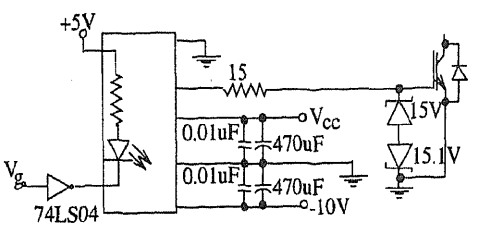


FIG. 10. Gate driver circuit.

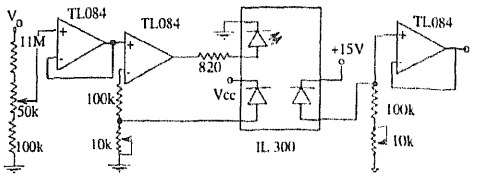


FIG. 11. Output voltage sensing circuit.

5.2. *Other Circuits*

The output voltage was sensed using a resistive divider, and isolation provided using a linear opto-coupler — IL300 [Fig. 11]. The switch ON-state drop was used to sense over current and subsequently disable pulse generation permanently, by latching a signal which inhibits the VCO [Fig. 12]. Over voltage protection was provided by temporarily inhibiting the VCO till the output voltage reduced below the set limit.

6. Experimental Results

The converter was tested at a low voltage, and power level up to nearly 500W, because of supply limitations in the laboratory. The IGBT used, Eupec FF150R10K, was a first generation IGBT, recommended for 15 kHz hard-switched operation, and had a very high output capacitance. This resulted in a lot of ringing at switch turn OFF, which limited the switching frequency of the converter to less than the desired value. The inductance of the resonant inductor (34 μH), used was substantially different from the required value (25 μH) which decreased the resonant frequency to 47.5 kHz.

The steady-state gain was measured by operating the converter in open loop and directly varying the VCO frequency. The input voltage used during testing was 35 V. The two values of load resistors used for testing were 100 Ω, and 125 Ω. The gains were found to be in close agreement with the theoretical one as shown in Figs. 13(a) & 13(b).

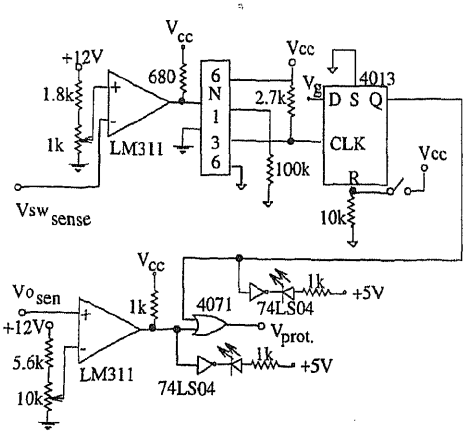


FIG. 12. Protection circuit.

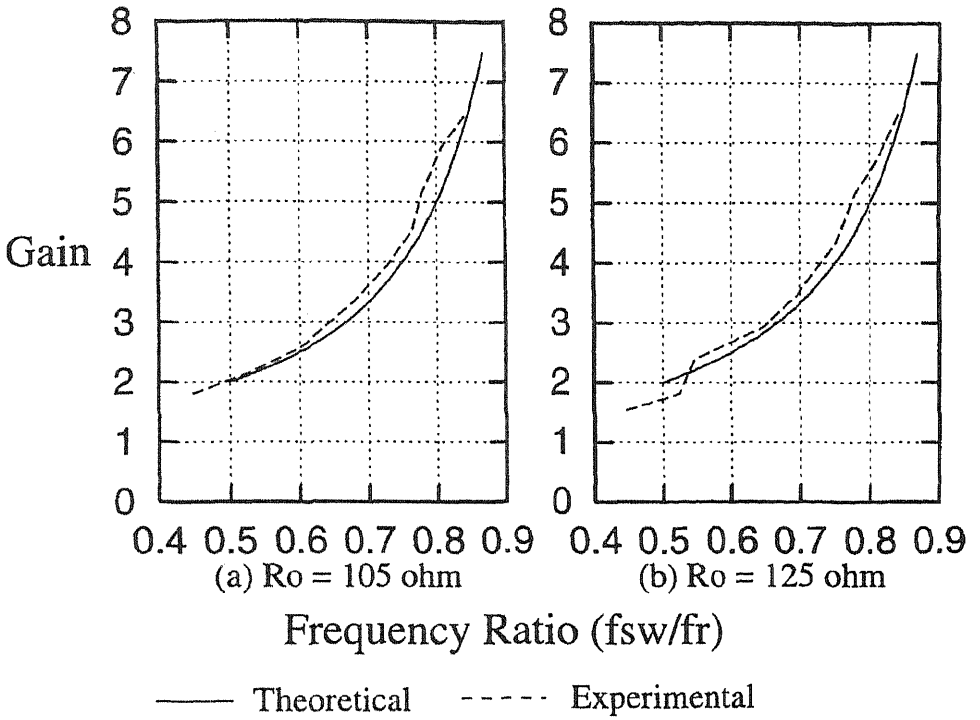
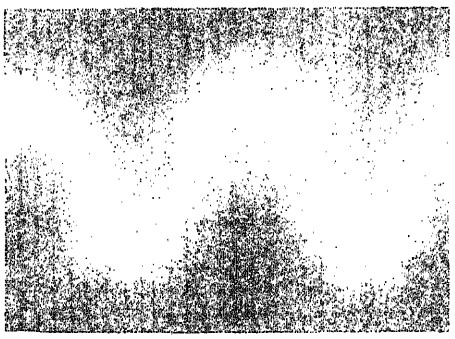
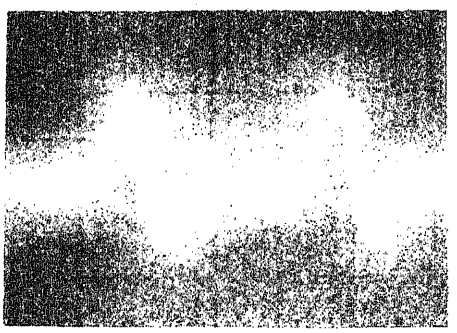


FIG. 13. Gain Vs. Frequency ratio.

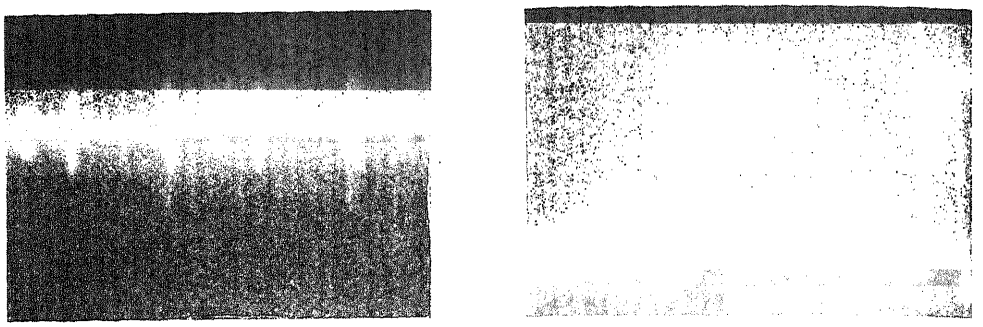
The various voltage and current waveforms [Fig. 14 (a) to 14(d)] were obtained for an input voltage of 36.9 V, and output voltage equal to 202 V. The resonant inductor current and the boost inductor current, however, were observed at lower voltages ($V_{DC} = 17.7$ V, $V_o = 31.7$ V). These are similar to the waveforms obtained from *SPICE* simulation [Sec. 4].



(a) 100 V/div, 5 us/div



(b) 0.8 A/div, 5 us/div



(c) 0.8 A/div, 5 us/div (d) 50 V/div, 5 us/div

FIG. 14. (a) Resonant capacitor voltage, (b) Resonant inductor current, (c) Boost inductor current and (d) Switch collector to emitter voltage.

7. Conclusion

A Quasi Resonant ZCS boost converter was designed, and simulated using *SPICE*. Device ratings and component values were determined using the simulation results. A modification was made in the basic topology and its operation, to make the circuit operation reliable during transient operation. The hardware implementation of the converter has been described in detail. Results of testing at low power level have been presented. The DC conversion ratio was found to be in close agreement with the theoretical one. The waveforms observed were found to match those predicted theoretically, and also those obtained from *SPICE* simulation.

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