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A new gate drive circuit for safe switching of MOS Controlled Thyristor (MCT)

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Abstract

The MOS Controlled Thyristor (MCT) is a relatively new class of MOS Gated Power Device having superior characteristics as compared to other similar type of devices. A new compact and reliable gate drive circuit for p-MCT has been developed having features of short-circuit/overcurrent and thermal protection along with low delay times and high immunity against spurious disturbances. The drive circuit has been tested in a chopper circuit upto 12.0 KHz with test under both short-circuit and thermal stress. Test results from a MCT based PWM controlled AC/DC converter using this drive circuit has also been presented.

Key words: 1. MCT, 2. Gate Drive, 3. Device Protection.,

Major discipline: Power Electronics Devices.

1. Introduction

The desired characteristics of high power semiconductor devices in switching applications are low forward voltage drop, high current capability, high voltage blocking capability at a sufficiently high frequency of operation. Recent developments in power semiconductor technology have made it possible to combine the advantages of fast switching, high voltage blocking capability along with high current conduction capability, in a single solid state device like the IGBT and MCT. Presently, the BiMOS power devices have already entered the field of high voltage power devices. The IGBT is a device, which has been accepted for medium-voltage application due to its simple gate drive operation and high switching speed. But for high power levels greater than achievable with IGBTs, other devices are to be considered. The GTOs are sometimes preferable devices because of its low voltage drop and high current conduction capability for its thyristor structure, but the drive circuit is much more complicated, as it is a current controlled device.

The MOS Controlled Thyristors, MCTs are a new class of device which combines the simple MOS gate drive with the thyristor on-state characteristics[1-3]. In other words, MCTs are a new BiMOS class of device which combines the thyristor current and voltage capability with MOS gated turn-on and turn-off. The main current conduction takes place through the bipolar structure, whereas, the turn-on and turn-off are controlled by the MOS structure. The bipolar power devices have high current and voltage capabilities as well as low on-state voltage drop. But they are slow because of the storage effects. On the other hand, the MOS power devices are very fast and because of their very high input impedance, they are relatively easy to drive. In

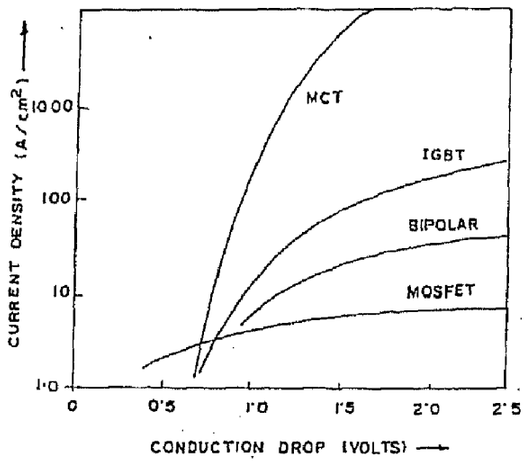


FIG. 1. Comparison of on-state voltage drop of different power devices.

fact, the MCT has the lowest on-state voltage drop for the same current density as compared to other power devices as shown in fig.(1). The essential features, which makes MCT superior to other power devices are listed below.

(1) They have high current and high voltage capability (e g, 1200 A and 2.5 kV), similar to bipolar.

(2) Very low forward voltage drop even at high current levels (e g, less than 1V).

(3) Very high input impedance, due to MOS input, like MOSFETs.

(4) Very high dv/dt capability, (e g, dv/dt>20kV/μs) which is much more than IGBTs.

(5) di/dt capability is very large, (e g, 20 kA/μs/cm^2).

(6) Turn-off current capability is very high, typically 120 A.

(7) Relatively high operating frequency, typically 20 KHz.

(8) Absence of Miller effect.

Thus it is observed, that for power levels which are not achievable with IGBTs, the MCT is the most preferred device in place of SCR and GTO.

The efficiency and reliability of a power converter depends on the switching efficiency of the power devices, which necessitates the use of suitable gate-drive circuit. Several MCT gate-drive circuits were reported by various workers in the past but most of them lacks the incorporation of in-built protection features in the same drive circuit. The gate drive designed by S. K. Sul *et al*[4]., for MCT uses a opto isolator and a buffering amplifier at the output. However, the gate drive designed by T. C. Lee *et al*[5]., contains a regular push-pull pair in parallel with a pair of power BJTs, so that the gate of MCT is driven by both the collectors of the power BJTs and the emitters of the signal transistors. A simple and efficient gate circuit has been proposed by J. Mathias[6]. Here, the control of the device is within the switching specification and ensures a homogeneous turn-on and turn-off of all the elements of the circuit, which ensures the device to

be exploited at its maximum capability. However, instead of using a continuous drive signal, a circuit has been proposed by S. Yuvarajan[7], which uses a pulse drive. In this circuit, the duty cycle and the pulse-width is controllable and the device characterisation results shows that the switching loss increases with pulse-width. An integrated drive chip (HIP 2030) having shut-down feature has also been reported by P. D. Kendle[8].

In this paper a new MCT gate drive circuit with in-built short-circuit and thermal protection features for safe switching of MCT has been presented. This circuit is much more versatile and compact and is particularly suitable for devices with ISOTOP packages. The circuit has been tested under normal condition and under fault operations and the various waveforms under these operating conditions are presented. Using the gate drive circuit, a PWM controlled MCT based AC/DC converter has been assembled, whose performance has been depicted in the oscillograms.

2. Operation of MCT, its short-circuit and thermal behaviour

Like other power device, a discrete MCT device is a parallel connection of a large number of typical MCT unit cells. The cross-sectional view of a typical p-MCT unit cell along with the various doping levels, have been shown in fig (2). If one examines this structure carefully, the equivalent circuit comes out to be the one as shown in fig (3). The operation of the MCT can be easily analysed if one considers this equivalent circuit as shown in fig (3).

From fig (3), a unit cell of a p-MCT consists of a thyristor, a NMOS transistor and a PMOS transistor. All the parallelly connected unit cells contain the NMOS OFF-FETs and only 5% of the cells contains the PMOS ON-FETs. When these PMOS are on, these unit cells are lathed-on, which initiates the lathing-on of the other cells. It may be noted that the lower n-p-n transistor (Q_2) has a wide and lightly doped base and hence, the collector-base junction gives high blocking voltage capability of the device. The upper p-n-p transistor (Q_1) has a narrow base and hence a larger α/compared to Q_2.

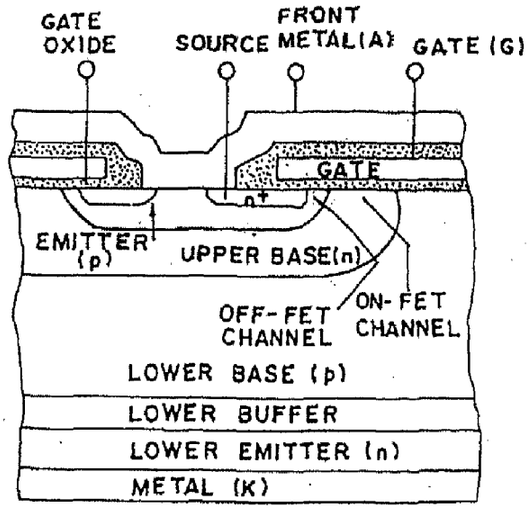


FIG. 2. Cross-sectional view of a p-MCT cell.

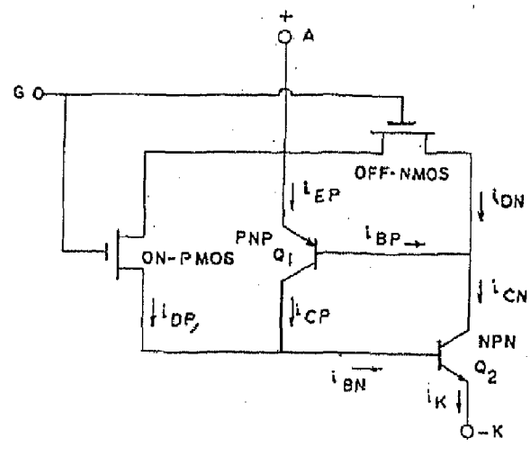


FIG. 3. Equivalent circuit of a p-MCT cell.

When no external current is injected into the base of either transistor, the device is OFF. When sufficient current is injected into the base of Q_2, by turning on the PMOS, such that the loop gain is unity, the MCT is turned on. This may be done by applying a typical negative voltage (-10V) at the gate of PMOS with respect to anode. The cumulative positive feedback thus generated, will drive the device into saturation. For a n-MCT, the gate voltage should be referred to the cathode.

When a positive gate voltage (+15V) with respect to the anode is applied, the NMOS is turned-on. Thus, the base-emitter junction of Q_1/is shorted. Hence, the current through the collector of Q_1 is diverted through the NMOS. This reduces the effective current gain α of Q_1 and hence the latching condition is broken. Since, the mobility of electrons are higher than that of the holes, the $r_{ds(on)}$ of NMOS is lower than PMOS. This ensures a higher turn-off current capability of the device.

2.1. *Thermal behaviour of MCT*

The temperature variation effects of MCT has been extensively done by C. V. Godbold *et al*[9]., covering a wide range of variation. The forward voltage drop of a MCT decreases with increasing temperature, due to the increase of lifetime of carriers. However, this decrease is marginally smaller for n-MCT than for p-MCT. Experimental results had revealed earlier that this decrease is about 0.2 V for a temperature increase from 50°C to 200°C in case of p-MCT.

The turn-on losses of MCT is negligible as compared to the turn-off losses. The turn-off loss of MCT is extremely high at temperature above 50°C due to the presence of long current tail because of increase of carrier lifetime. This turn-off loss for MCT is the highest among the other classes of MOS-gated devices. For example, the MCT turn-off loss is almost 3 times at 50°C and 4 times at 100°C as compared to a similarly rated IGBT. However, it is quite interesting to note that, the two stage current fall, which originates the current tail, disappears for temperature below 0°C, thus minimizing turn-off loss at lower temperature. The higher turn-off switching loss may have a cumulative effect if proper heat sink is not provided, thus leading to permanent destruction of the device, due to over temperature. So, it is a safe approach to incorporate a temperature protection feature in the gate drive circuit of a MCT. It has been observed that the peak turn-off current (I_{off}) of a MCT decreases with temperature.

2.2. *Short circuit behaviour*

During turn-off of a MCT, the latching condition is broken by directing the path of the holes through the NMOS transistor. If the anode current is too large, the gate control becomes ineffective, which can lead to permanent destruction of the device, owing to permanent latch-up. The short-circuit/overcurrent behaviour MCT were studied by J. Mathias *et al*[6]., by placing a IGBT in series to protect the MCT under fault current operation. The commutation of this IGBT is so adjusted that it does not interfere with the operation of MCT. If the anode current is above the commutation capability of the device, then at the instant the device is turned-off by the gate pulse, the anode current initially falls and then rises due to the latch-up phenomena. So, in designing a good gate drive circuit, one must take care of protecting the device under any short circuit or overcurrent operation.

3. Drive requirements

Some of the essential key points that should be considered when designing gate drive circuits for MCT are:

(a) The speed at which the device latches is dominated by the SCR turn-on time. Gate drive speed has no effect on the turn-on speed.

(b) The magnitude of the turn-on gate voltage, does not change the on-state voltage of the MCT.

(c) Although the turn-off of the MCT is initiated by the NMOS, the actual turn-off time is dominated by the carrier recombination.

(d) If the gate bias is not maintained during off-state, the device is susceptible to spurious turn-on due to high dv/dt and high input impedance of the gate.

By considering the equivalent circuit of a MCT as shown in fig (3), it is seen that it consists of two basic blocks (a) the SCR and (b) the PMOS and NMOS. The main conduction current of the MCT takes place through the SCR section whereas the commutation of the device is achieved by initiating the MOSFETs. By applying a negative voltage at the gate with respect to the anode, the MCT is turned-on and by applying a positive gate voltage, the MCT is turned-off. Generally, the magnitude of the positive turn-off voltage is higher than the magnitude of the negative turn-on voltage. This ensures faster turn-off at higher current, since the turn-off is initiated by the NMOS transistors. Typically, the gate voltages for turn-off is +15V and turn-on is −10V. Moreover, for faster turn-off of the device, the gate to anode capacitance (~10 nF) has to be charged at a faster rate. This implies a faster rise-time of nearly 200 ns of the gate voltage with a higher gate charging current of 2A, during turn-off. ,

4. Proposed MCT gate drive circuit

The new gate drive circuit proposed in this work has in-built features like short circuit/over-current protection, thermal shutdown and fault sensing within a single circuit, thus making it more versatile, reliable and compact. This circuit has been designed by taking into consideration the different drive requirements as discussed in the previous section. This circuit has a high immunity towards spurious disturbances in addition to low delay times and operation over a relatively wide range of frequency.

4.1. *Operation under normal condition*

The operation of the drive circuit can be best understood by considering the circuit diagram shown in fig. (4). The input stage is a isolation stage between the low voltage control part and the relatively high voltage drive part, which has been achieved by a fast switching optocoupler OP1. The necessary drive polarities of the MCT has been achieved by some high frequency bipolar transistor stages. When the input at the base of transistor Q_c is low, the voltage at B and E is also low. Initially, the fast switching diode DS is non-conducting. In this condition, the output of the comparator U1 is high. Thus, the base of transistor Q_6 is low and hence it is non-conducting. As Q_4 and Q_5 constitute a totem-pole output, the gate of the MCT is high and hence it is in off-state. When the input of OP1 is high, the voltage at point F does not become imme-

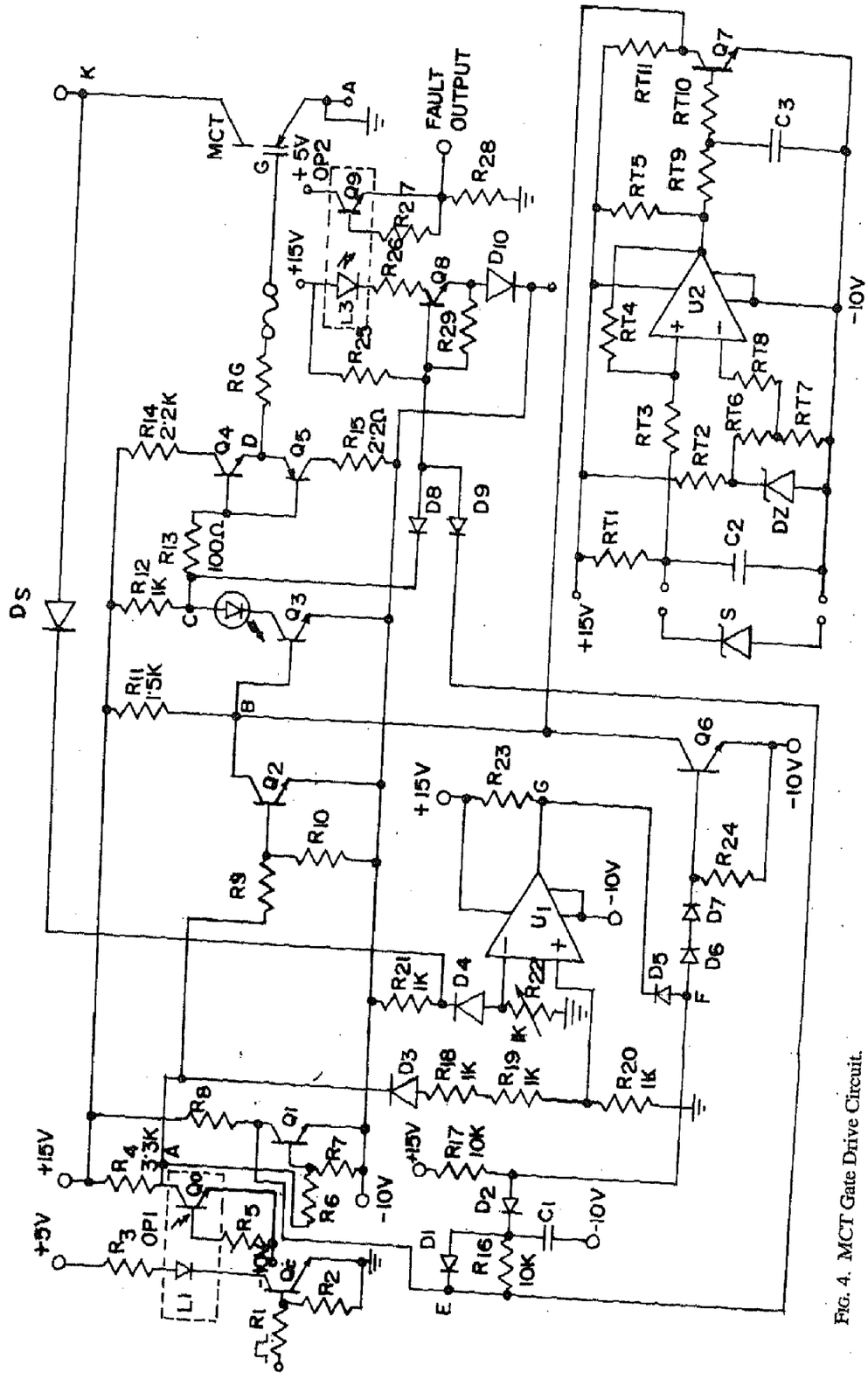


FIG. 4. MCT Gate Drive Circuit.

diately high, due to the presence of R16 and C1 delay network. So, Q_6 still remains in the cut-off state although the voltage at G is high. Since, the voltage at C is low, the MCT now turns on and the diode DS becomes conducting, thus clamping the inverting terminal voltage of U1 to the cathode voltage (small negative value) of the MCT. Hence, the output of U1 goes from a high state to a low state. After sometime, determined predominantly by R16 and C1 combination, (although R8 and R17 will also affect the delay) the voltage of the collector of Q_1 becomes high but the voltage at G remains in low state. If this small delay time was not given, the collector of Q_6 would become low, thus preventing any transmission of pulses. Hence, it is necessary to have a small delay for the operation of this circuit.

4.2. *Operation under fault condition*

During the event of any short circuit/overcurrent operation, the voltage at cathode terminal of MCT becomes increasingly negative. This makes the comparator U1 output terminal to a high state. As the voltage at E and G are both high, the transistor Q_6 is switched-on, thus pulling own to voltage at B to a low value. Hence, the voltage at D becomes high and the MCT is turned-off. As during short circuit or overcurrent, the voltage at the inverting terminal of the precision comparator U1 is compared with a predetermined value, the value of the device current at which the device has to be shut down can be easily set by adjusting either R20 or R22. Since, the short-circuit or overcurrent protection is done by voltage sensing principle at the cathode terminal, no lossy current sensing element is required which eventually eliminates any unwanted noise in the circuit.

The device temperature is constantly sensed by a small IC sensor (S) mounted on the heat sink, during normal operation of the circuit. This value is compared with a preset value by a fast switching comparator (U2) having a positive feedback. If the temperature of the MCT becomes abnormally high, the output of U2 goes high, which drives transistor Q_7 into saturation. Hence, the voltage at D becomes high (+15V) and the MCT is turned-off to prevent permanent destruction of the device.

When any of the two faults occur, the voltage at nodes E and C becomes simultaneously high. This produces an isolated "FAULT" signal by the optocoupler OP2. This signal can be fed to control block of the application for taking necessary decisions at the control logic level or for total equipment shutdown. The LED shown by I2, will glow during normal transmission of pulses and will be off for any fault operation.

5. Experimental results

The proposed gate-drive circuit has been tested in a simple chopper circuit with a inductive load. The MCT used in this measurement is a p-MCT (MCTA60P60 of Harris Semiconductor), whose specification are given in Appendix. The oscillograms in the figures show the different waveforms for a dc voltage of 70V for both under normal and short circuit operation. A simple polarised RC snubber circuit has been used in the power circuit. Fig. (5a) and fig. (5b) shows the MCT gate voltage and the MCT cathode voltage with respect to the common anode terminal during turn-on and turn-off under normal operation. The overall turn-on and turn-off delays at 2.5 kHz has been measured and found to be 1.8 μs. and 0.7 μs respectively. It has been also observed that this delay is mostly contributed by the isolating optocoupler. The voltage at the

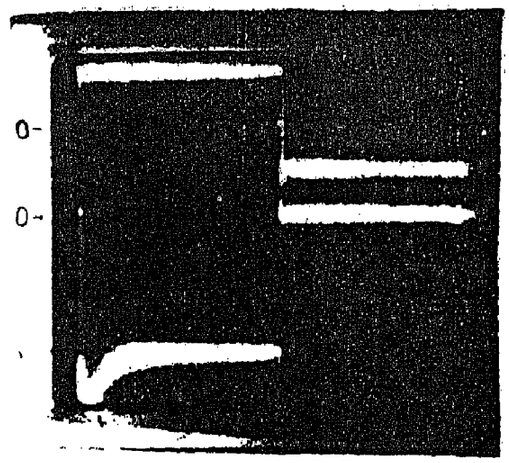


FIG. 5a. Turn-on switching – Upper : V_{GA}(10V/div); Lower : V_{KA}(20V/div); Time : 50 msec/div.

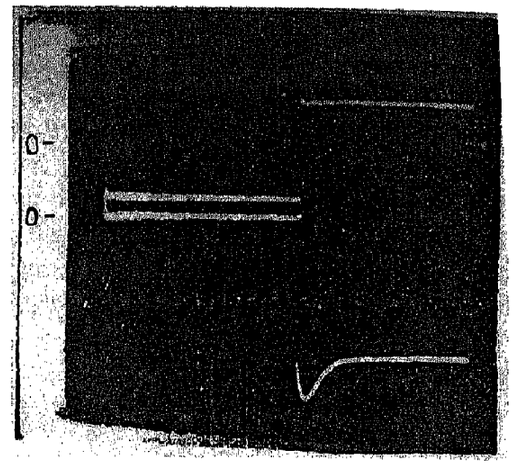


FIG. 5b. Turn-off switching – Upper : V_{GA}(10V/div); Lower : V_{KA}(20V/div); Time : 50 msec/div,

input of the drive circuit and the MCT device current under normal operation is shown in fig. (6), from which a current tail is observed.

The same drive circuit was also tested under short-circuit/overcurrent operation in the same chopper circuit. Fig. (7a) shows the waveform of the gate to anode voltage and the device current during short circuit operation. It is noticed from this figure that small voltage spikes at the gate voltage of 0.1 μs. duration is present, which is necessary for the operation of this circuit. The waveforms for the input drive and the device current has been shown in fig. (7b) during short circuit stresses. It is observed that although the gate drive is present under short-circuit operation, the cathode current initially rises during the blind period and then falls-off sharply with a current tail at the end. The temperature shut-down capability has been tested and the operation has been found to be satisfactory. Measurements were also carried out over a wide range upto 12.0 KHz and the performance has been found to be satisfactory.

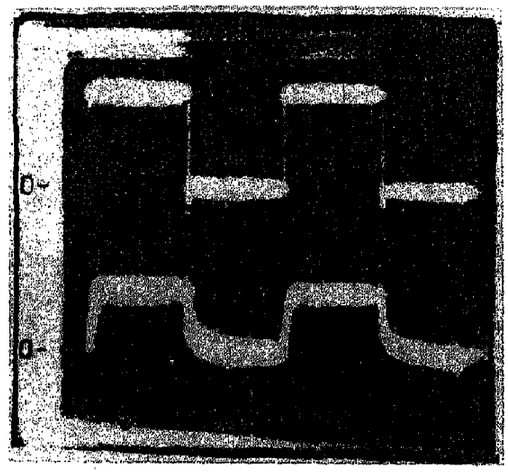
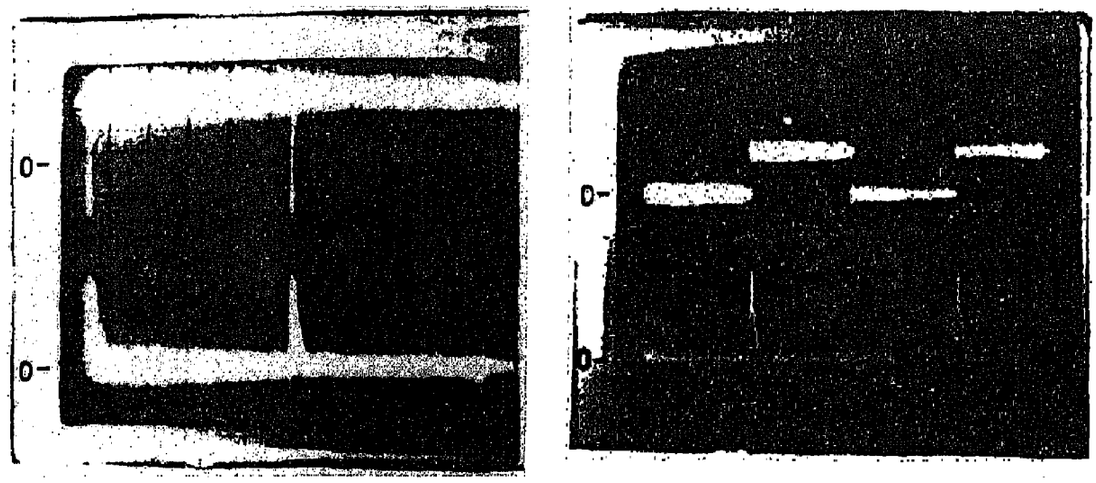


FIG. 6. MCT current response to input signal – Upper : Input (2V/div); Lower : I_A (10A/div); Time : 100 msec/div.



(a) (b)

FIG. 7. Operation of the drive circuit during short-circuit condition. (a) Upper : V_{GA}(10V/div), Lower: I_A(10A/div), Time : 100 msec/div; (b) Upper : Input(5V/div), Lower : I_A(10A/div), Time : 100 msec/div,

Since, MCTs are voltage control devices, they are suitable for PWM applications. As an application of the proposed gate drive circuit, a MCT based half-controlled three phase AC/DC converter has been assembled, for DC drive application. The PWM control pattern is a seven pulse scheme where the central and the end pulses have a width of β and β/2 respectively, where β is the modulation index. The intermediate pulses have pulse width of xβ where the

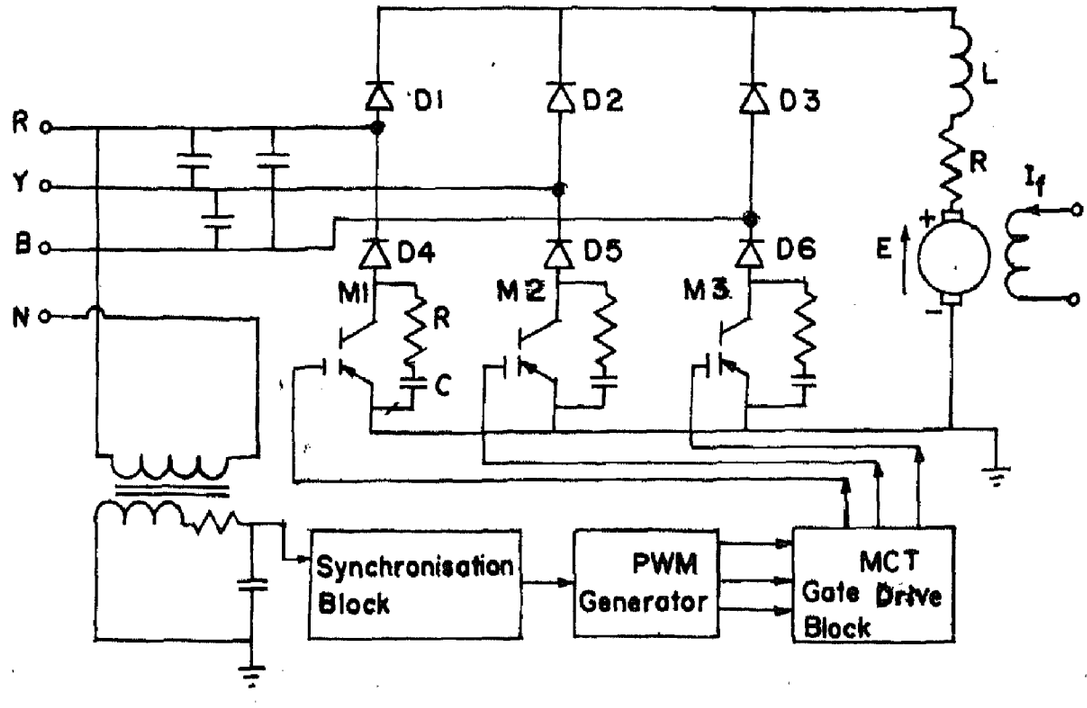
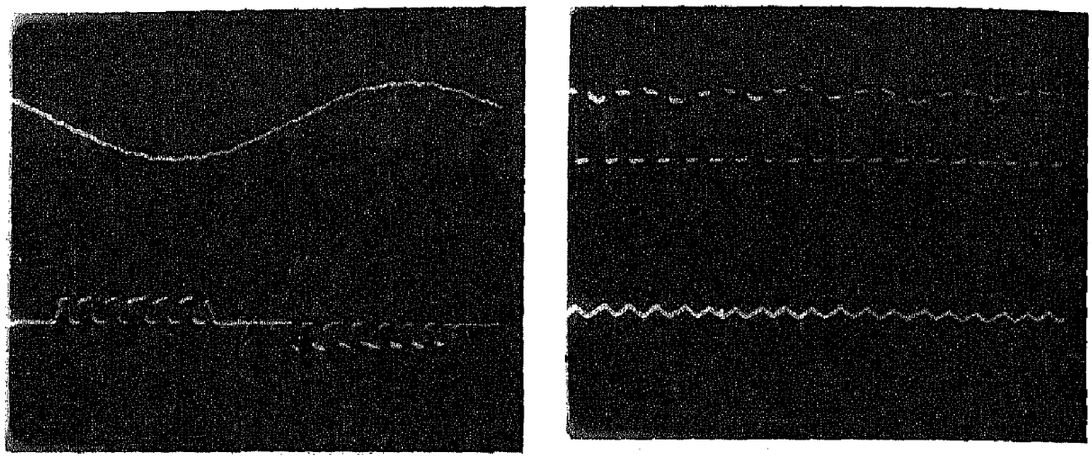


FIG. 8. Schematic diagram of the PWM AC/DC converter circuit using MCT.



(a) (b)

FIG. 9. Input and output waveform of the MCT based AC/DC converter circuit. (a) Upper : V_{LL}(100V/div); Lower : Input current(5A/div); Time : 2 msec/div; (b) Upper : Output voltage (50V/div); Lower : Output current (5A/div); Time : 2 msec/div.

value of x is optimised to a certain fraction, such that the lower order input current and output voltage harmonics are simultaneously minimum. In the power circuit, as shown in fig. 8, the three MCTs form the lower half of the bridge and the anodes are common, thus avoiding any need of isolated drive. Apart from the three upper-half diodes of the half-controlled scheme, three additional diodes are added in series with the MCTs, as these present devices do not have reverse blocking capability. The necessary control patterns for gating the MCTs are generated from line-synchronised control logic block, which is then fed to the respective gate drive circuit of the MCT through the optocoupler. Sample oscillograms of the input and output waveforms taken from this converter are shown in fig. (9a) & fig. (9b) for a modulation index of 0.5.

6. Conclusions

The operation, short-circuit & thermal behaviour and essential drive requirements of a MCT has been briefly reviewed. The necessity of short-circuit and thermal protection needed in a drive circuit for efficient and safe switching of the MCT has been highlighted. A new gate drive circuit, which is more versatile and compact, including the features of short-circuit and thermal protection, has been presented. The use of any differentiating and latching element in the circuit has been avoided, thus making the circuit more immune towards spurious disturbances in addition to low delay times. Experimental results have revealed the operational range of frequency of the circuit to be relatively wide. Under the event of any fault operation (short-circuit or thermal), the circuit senses the fault quickly and after turning-off the device, a 'FAULT' signal is send to the control block of the system. The above gate drive circuit has been tested in a chopper circuit as well as in a PWM AC/DC converter circuit and the performance has been found to be within expectations.

7. Acknowledgements

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APPENDIX

Maximum rating of MCTA60P60

Peak off-state voltage	:	–600 V
Average on-state current	:	60 A,
Peak controllable current	:	120 A,
Peak gate voltage	:	±20 V,
dv/dt	:	1000 V/μsec,
di/dt	:	500 A/μsec,
On-state voltage at $V_{GA} = -10V$	:	–1.5 V,

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