J. Indian Inst. Sci., Nov.–Dec. 1997, **77**, 535–554.

An evaluation of control schemes for a hvdc system feeding into a weak ac system

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Abstract

An evaluation of steady-state stability boundaries various control schemes at the inverter terminal of a hvdc system feeding into weak ac system has been reported here. The stability analysis has been performed using root locus technique. The influence of the sending and the receiving ac system impedance on the system stability boundaries has also been determined. It is observed that proper optimization of controller parameters may provide the same setting time or system damping.

Since it is a well established fact that the minimal reactive power demand, and the harmonics generation are the salient features of the extinction angle control. Hence, it is not desirable to operate the hvdc system with other control schemes during steady-state. However, the extinction angle control may cause voltage/power instability during transients. Hence it is required to operate the hvdc system with another control scheme during transients. This paper also deals with effects of switching among control schemes for improving system performance. It has been observed that the switching among the control schemes may be achieved successfully and the dynamic overvoltages of the system may be minimized using the ac or the dc control scheme. The effectiveness of various control schemes has been determined by introducing each control scheme just after the faults for 300 ms and then reverting the system operation to the extinction angle control. It is also observed that switching among control schemes does not cause instabilities.

1. Introduction

The steady-state stability of an hvdc system is investigated to determine the stability boundaries of various inverter controls. The influence of the system and controller parameters on the stability boundaries is also investigated. These studies will be useful in determining the control system response for a given system configuration and in providing information about the controller design for various operating ranges.

A simplified model of an hvdc system has been used to design current control with an assumption that the ac bus voltage at the inverter does not change significantly [1] and [2]. This assumption is valid only if the inverter is feeding into a strong ac system. If the receiving ac system impedance is relatively high, the basic assumption of constant ac voltage in [1] and [2] is invalid. This assumption was dropped in the study reported in references[3–6]. These studies have not included details of the compensator and integral control. Hence, the results obtained in references[3–6] are of not very great practical significance. furthermore, the scope of these studies is limited only to the extinction angle control on the inverter terminal.

The technique presented in this paper overcomes the above-mentioned drawbacks. In addition, the following control modes at the inverter terminal are also incorporated.

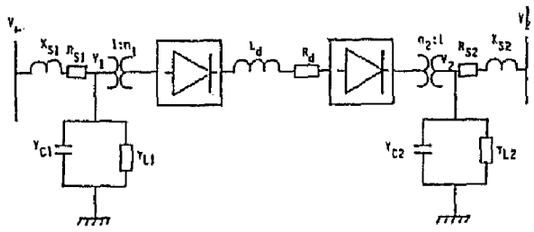


FIG. 1. Model of simplified system used for the stability analysis.

Base Case System Parameters

Sending AC System					*Receiving AC System*				
SCR	R_{s1} (Ohms)	X_{s1} (Ohms)	Y_{C1} (Ohms)	r_{L1} (Ohms)	SCR	R_{s2} (Ohms)	X_{s2} (Ohms)	Y_{C1} (Ohms)	r_{L2} (Ohms)
4.0	0.5	5.7	0.0045	10^{18}	1.5	7.8	36.57	0.0080	10^{18}

Effective Inductance of DC Links = 2.5 Henry
Effective Resistance of DC Links = 1.5 Ohms
Line to Line Voltage at the Inverter AC Bus = 230 kv
Line to Line Voltage at the Rectifier AC Bus = 138 kv
Base Value of Controller Gain = 5.0
Base Value of Controller Time Constant = 0.8

(a) Extinction angle control,
(b) Power factor control,
(c) DC voltage control,
(d) Reactive current control, and
(e) Reactive power control.

The digital simulation is carried out to further investigate the system recovery from various faults for different control schemes. There are various techniques available in the literature for simulating hvdc systems in detail on a digital computer[7-9]. However, the use of the EMTP and EMTDC packages has become more popular because of their versatility and user friendliness[10-12]. These simulation studies of hvdc systems are limited to conventional control modelling at the inverter terminal of the hvdc system. This paper is devoted to the modelling of the hvdc system and its various control schemes using the EMTDC package for digital simulation.

2. System model and equations

The following assumptions are made to determine the steady-state stability boundaries of an hvdc system. The system considered for the study is shown in Figure 1.

Sending End:

i) The ac system of the rectifier is supplied by an infinite source. That is, the capacity of the system is much larger than that of the hvdc transmission. Hence, the voltage on the ac bus can be considered to be constant.

ii) The ac system is represented by an equivalent machine. This equivalent machine is represented by a voltage source behind the machine transient impedance.

iii) The time constants of the excitation system are much larger than those of the dc system. Hence the dynamics of the excitation system are ignored.

iv) The ac voltage is balanced and contains no harmonics. This implies that the filters absorb all harmonics generated by the dc system.

Receiving End:

i) An equivalent generator represents the receiving ac system.

ii) The impedance of the receiving ac system is represented by an equivalent series connection of lumped resistance and reactance (R_{S2}, X_{S2}).

iii) A single capacitor (C_2) represents the capacitance of the ac system and the compensating equipment. The reactie power of loads can be considered as a reduction in the value of this capacitor.

iv) The total L_d and R_d represent inductance and resistance, respectively, of the dc line and the smoothing reactors on both sides.

The system shown in Figure 1 is used for investigating the steady-state stability of an hvdc system.

$$V_{1\infty}^2 = (V_1 + \Delta V1)^2 + (DV_1)^2$$

$$= \frac{\left(V_1 + (P_1 + P_{L1})R_{S1} + (Q_1 + Q_{L1})X_{S1}\right)^2}{V_1} \tag{1}$$

where, $V_{1\infty}$ = rms value of the generating station bus voltage
V_1 = rms value of the rectifier bus voltage
P_1 = $V_1 I_1 \cos \phi_1$
P_l = V_1^2 / r_{L1}
Q_1 = $V_1 I_1 \sin \phi_1$
Q_{L1} = $-\omega C_1 V_1^2 = -Y_{C1} V_1^2$
I_1 = $\sqrt{3}$ x fundamental current component of the ac side current
$\cos \phi_1$ = power factor at the rectifier terminal

Equation (1) is further simplified to the following relationship by substituting expressions of the active and reactive power.

$$V_1^2\infty = F_1 V_1^2 + 2V_1 I_1 (\cos\phi_1 + D_1 \sin\phi_1) + Z_{S1}^2 I_1^2 \tag{2}$$

where,

$$F_1 = \left(1 + \frac{R_{S1}}{r_{L1}} - X_{S1} Y_{C1}\right)^2 + \left(\frac{X_{S1}}{r_{L1}} + R_{S1} Y_{C1}\right)^2$$

$$Z_{S1} = \sqrt{R_{S1}^2 + S_{S1}^2}$$

$$C_1 = R_{S1} + \frac{Z_{S1}^2}{r_{L1}}$$

$$D_1 = X_{S1} - Y_{C1} Z_{S1}^2$$

During steady-state, the power factor is defined as follows [5].

$$\cos\phi_1 = \cos\alpha - \frac{X_C I_d}{\sqrt{2} V_1 n_1} \tag{3}$$

$$I_1 = \frac{3\sqrt{2}mn}{n} I_d = K_R I_d \tag{4}$$

where,

X_{C1} = communicating reactance at the rectifier terminals

α = firing angle

n_1 = transformation ratio (secondary to primary side)

m = no. of bridges connected in series

I_d = direct current in the dc system

The linearized version of equation (2) is given below.

$$\Delta V_1 = -f_{dr}\Delta I_d - f_{\alpha r}\Delta_\alpha \tag{5}$$

where,

$$f_{dr} = \frac{f_2}{f_1}; f_{ar} = \frac{f_3}{f_1}$$

$$f_1 = F_1 V_{10} + K_R I_{do} C_1' \cos\alpha_o + \left(D_1 K_R I_{do}\right)\left(\frac{K_R V_{10} - V_{do}\cos\alpha_O}{V_{ds}}\right)$$

$$f_2 = K_R Z_{S1} I_{do} + C_1\left(V_{do} - R_e I_{do}\right) + D_1'\left(V_{ds} + \frac{R_e I_{do} V_{do}}{V_{ds}}\right)$$

$$f_3 = K_R V_{10} I_{do} \sin\alpha_O\left(D_1'\frac{V_{do}}{V_{ds}} - C_1\right)$$

$$R_{er} = \frac{3}{\pi} X_{cr}$$

$$V_{do} = K_R V_{10} I_{do}\cos\alpha_O - R_e I_{do}$$

$$V_{ds} = \sqrt{(K_R V_{10})^2 - V_{do}^2}$$

The subscript "*o*" represents the steady-state value of the variables.

Similar equations are obtained at the inverter end.

Modelling of DC Link

The following equation represents the dc link.

$$L_d \frac{dI_d}{dt} + R_d I_d = V_{dR} - V_{dI} \tag{6}$$

where,

$$V_{dR} = K_R V_1 \cos\alpha - \frac{3}{\pi} X_{ci} I_d$$

$$V_{dI} = K_1 V_2 \cos\beta + \frac{3}{\pi} X_{ci} I_d$$

The incremental equation of the dc link is written as below.

$$(T'_d S + 1) I_{do} = \Delta\alpha + H_\beta \Delta\beta \tag{7}$$

where,

$$H_\alpha = \frac{-d_2}{R_d - d_1}, \mathrm{H}_\beta = \frac{d_3}{R_d - d_1}, T'_d = \frac{L_d}{R_d - d_1}$$

$$d_1 = K_i f_{di}, \cos\beta_o - K_R f_{dr} \cos\alpha - (R_e + Re_i)$$

$$d_2 = K_R (f_{\alpha r} \cos\alpha_0 + V_{10} \sin\alpha_0)$$

$$d_3 = K_I (f_{\alpha i} \cos\alpha_0 + V_{10} \sin\alpha_0)$$

Development of block diagram and characteristic equation

Constant Extinction Angle (CEA) Control:

In steady -state, the relationship among β, γ, and direct current is given as follows:

$$\cos\beta = \cos\gamma - \frac{\sqrt{2}\, X_{ci}}{V_2 n_2} I_d \tag{8}$$

where,

β = ignition angle

γ = extinction angle

X_{ci} = commutating reactance at the inverter bus

V_2 = the inverter bus voltage (rms)

n_2 = transformation ratio

The incremental equation is

$$\Delta\gamma = S_2\, \Delta_\beta - S_1\, \Delta I_d \tag{9}$$

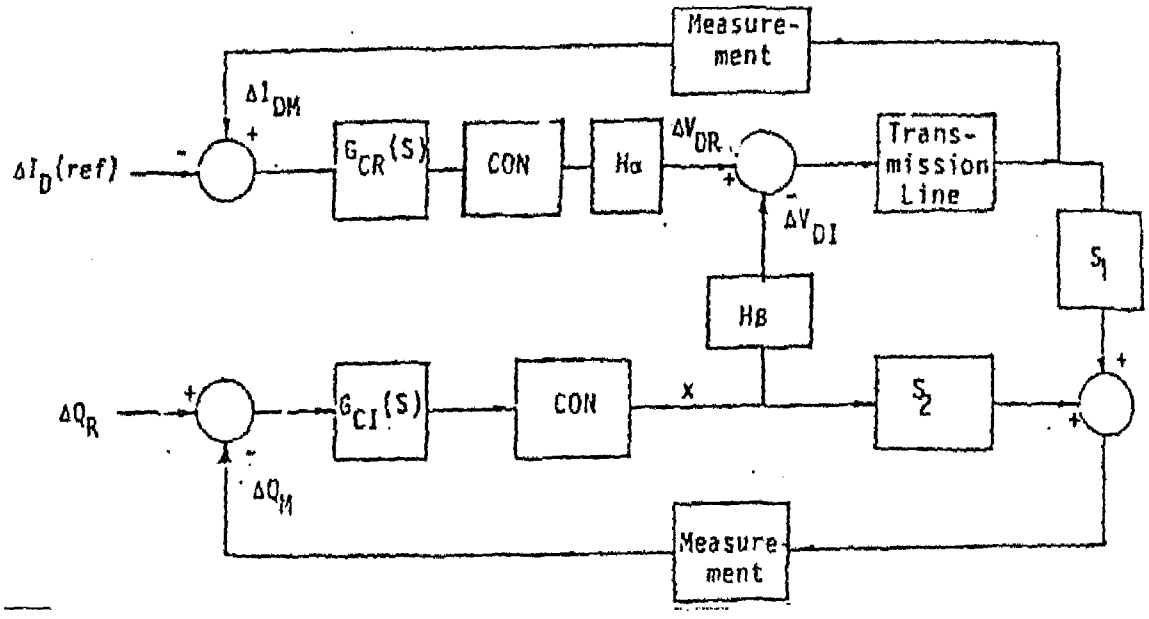


FIG. 2. Block diagram for stability analysis of various control schemes.

where,

$$S_1 = \frac{\sqrt{2}x_{ci}}{V_{20}Sin\gamma_0} \quad (1+\frac{f_{dI}I_{d0}}{V_{20}})$$

$$S_2 = \frac{1}{\sin\gamma_0}\left(\sin\beta_0 - \frac{\sqrt{2}f_{\alpha i}X_{cI}I_{do}}{V_{20}^2}\right)$$

Using equations (7) and (9) , the block diagram of the complete system is obtained as shown in Figure 2. This block diagram is used to determine the steady-state stability of the hvdc system operating with various control schemes at the inverter terminal. The root locus technique is used to determine the stability of the system as it has been used successfully in the part[1-2].

The controller configuration at the rectifier and the inverter has been considered as follows.

$$G_C(S) = \left(\frac{sK_P + K_I}{S}\right)\left(\frac{1+T_a s}{1+T_b s}\right) \tag{10}$$

The converter is represented by the following transfer function:

$$T(s) = \left(\frac{1}{1+T_{de}s}\right)$$

Final form of characteristic equation can be written as follows by substituting for the converter model and controllers transfer function from equation (10) .

$$(1 + T_d' S)\,(1 + T_f S)\,(1 + T_{f1} S)\,(S)\,(1 + T_{b2} S)$$

$$(1 + T_{de2} S)\,(1 + T_{b1} S)\,(1 + T_{de1} S)\,(S) + S_2 K_1$$

$$(1 + T_d' S)\,(1 T_d' T_{fS})\,(K_{I2} + K_{p2} S)\,(1 + {}_{a2} S)\,(S)$$

$$(1 + T_{b1}S)\,(1 + T_{de1}S) + S_1\,H_\beta\,K_1\,(1 + T_fS)$$
$$(K_{I2} + K_{p2}S)\,(1 + T_{a2}\,S)\,(S)\,(1 + T_{b1}S)\,(1 + T_{de1}S)$$
$$+ K_O\,H_\alpha\,(1 + T_{f1}S)\,(K_{I1} + K_{p1}S)\,(1 + T_{a1}S)\,(S)$$
$$(1 + T_{b2}S)\,(1 + T_{de2}S)\,(S) + K_O\,K_1\,H_\alpha\,S_2$$
$$(1 + T_{a1}S)\,(1 + T_{a2}\,S)\,(K_{p1}S + KI_1)$$
$$(K_{p2}S + K_{I2}) \tag{11}$$

The characteristic equation the various controls remains the same as equation (11) but the value of S_1 and S_2 change. The expressions for S_1 S_2 for various control schemes may be derived by relating among the $\Delta\beta$, Δ Id and control scheme.

3. Discussion

The influence of the system and controller parameters on system stability are discussed next the following controller configuration is implanted the inverter terminal.

$$= K_C\left(\frac{T_Cs+1}{s}\right)\left(\frac{1+T_as}{1+T_bs}\right) \tag{21}$$

where K_C = controller gain

T_C = controller time constant

T_a, T_b = time constant of the lead-lag network

The Influence of Controller Gain on the System Stability

The sending ac system and the receiving ac system impedance's are fixed to that the ac systems of the receiving end and the sending end have short circuit ratios of 4.0 and 1.5. The dc line time constant is fixed to 0.167. This system data is used for the base case. The basic reason for choosing the low short circuit ratio for the inverter ac system is that it causes larger voltage fluctuations and can cause voltage and power instability. Consequently, the controller must be designed to achieve good performance for these operating conditions. The distributing dc line will be considered for digital simulation. Hence, the equivalent induction and resistance is considered here so as to produce the same time constant as of the distributed dc line.

The influence of the controller gain in the range 5.0 to 25.0 is shown in Figure 3. The most sensitive roots of the characteristic equation are plotted in Figure 3. The following conclusions are drawn :

a) As the controller gain increases, the system becomes less stable for various control modes.

b) It is possible to obtain the same settling time for all control modes but for different gains.

c) The system damping for all ranges of gain is less than 0.707. Hence, to achieve a system damping greater than 0.707, the controller gains need to be reduced. However, lower gain values may produce sluggish response.

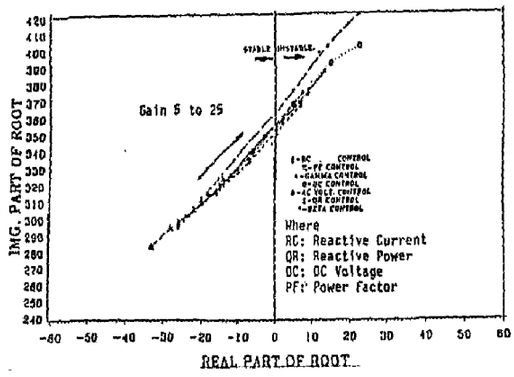


FIG. 3. Influence of controller gain of various control schemes at the inverter on the dominant roots.

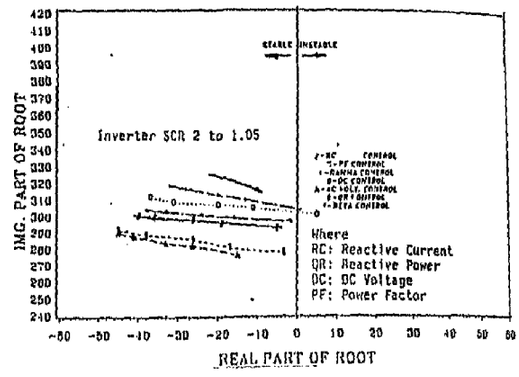


FIG. 4. Influence of the receiving AC short circuit ratio on the dominant roots.

The Influence of receiving AC System's Short Circuit Ratio of the System Stability

The controller gain for all control modes is fixed to 5.0 so that a sufficient stability margin is available to study the effect of the receiving ac system's short circuit ratio. The receiving end short circuit ratio is varied from 2.00 to 1.05 to investigate its influence on stability. The reason for selecting these values of short circuit ratio is to determine the stability of the system around the base case of short circuit ratio of 1.5. The dc line time constant is fixed to its base value of 0.167. The movement of the most sensitive roots is shown in Figure 4. The following conclusions are drawn:

a) As the short circuit ratio of the receiving ac system is reduced, the system response deteriorates and the system tends to become unstable.

b) The controller gain must be lowered as the short circuit ratio of the receiving end reduces to achieve the desired response.

c) The degree of stability varies for different control modes. However, it can be forced to be the same by proper adjustments of gains as discussed in the previous section.

The Influence of the Sending AC System's Short Circuit Ratio on the System Stability

The receiving ac system impedance, dc line impedance, and controller gain are fixed to base values. The sending ac system impedance is varied to obtained short circuit ratio 1.0 to 88.0. These numbers of short circuit ratios are chosen to represent very weak to very strong ac systems. Hence, this study will indicate the trend of stability with in the two extremes.

The movement of the most sensitive roots is illustrated in Figure 5. It is observed from Figure 5 that as the short circuit ratio of the sending end decreases, the system becomes more stable. This is because the rise in the direct current is controlled by the sending end impedance.

4. Modelling of AC-DC-AC system using emtdc package

Power system dynamics is simulated in the time domain with three phase representation of an ac network in the EMTDC package. Subroutines are available to model frequency dependent distributed transmission line, generalized six-pulse thyristor bridge with damping circuits, trans-

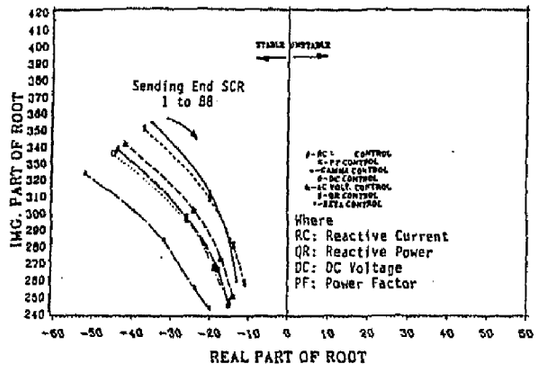
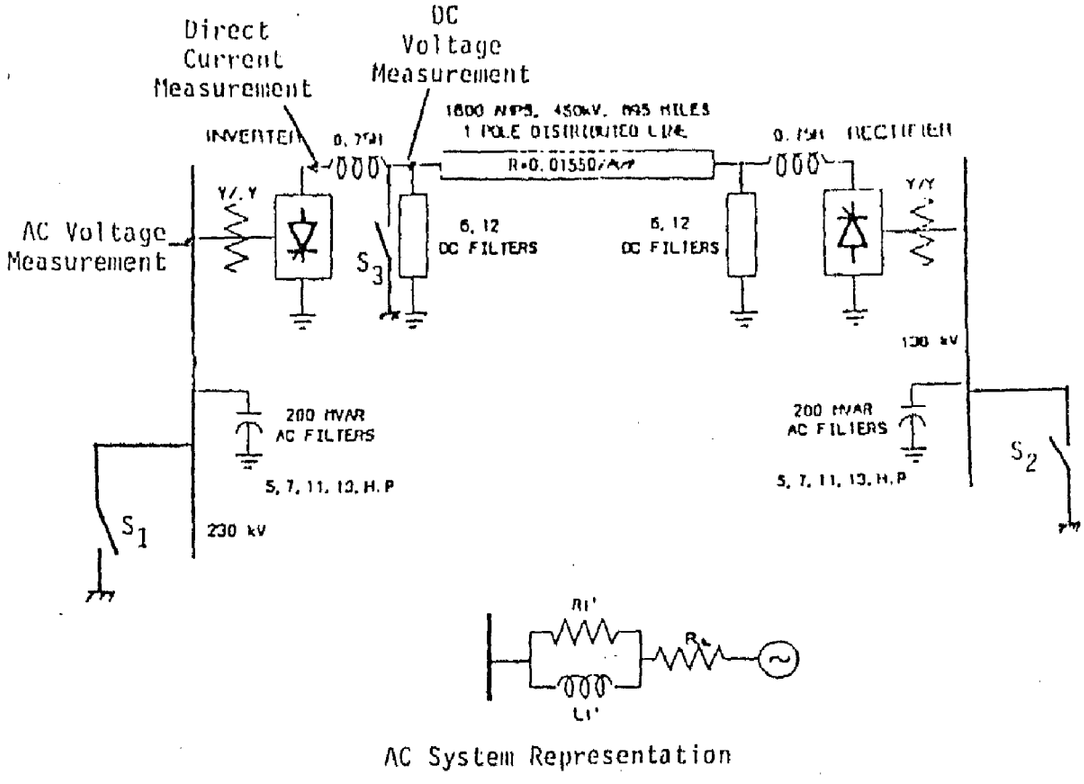


FIG. 5. Influence of the sending AC system short circuit ratio on the dominant roots.

former saturation, metering system, and the dc conventional controls. New computer pragrams are developed and implemented to realize the various control modes at the inverter terminal.

The point to point ac-dc-ac system shown in Figure 6 is modelled and simulated to investigate the system recovery from various faults for different control schemes. The system with the following specifications at the inverter is modelled.



S_1: Switch is closed to apply the ac faults at the inverter ac bus.
S_2: Switch is closed to apply the ac faults at the rectifier ac bus.
S_3: Switch is closed to apply the dc fault at the inverter terminal.

FIG. 6. A HVDC system used for investigations.

Table 1(a)
Data for the Receiving AC System

SCR	R1 (Ohms)	R2 (Ohms)	L2 (Henry)	Z Mag (Ohms)	Z Angle (deg)	SCP Mag. (MVA)	SCP Angle (deg)	L-L, Voltage (kv)	Filter Ratings (MVAR)
1.5	5.2074	523.81	0.0975	37.385	78	1415	78	230	200

Table 1(b)
Data for the Sending AC System

SCR	R1 (Ohms)	R2 (Ohms)	L2 (Henry)	Z Mag (Ohms)	Z Angle (deg)	SCP Mag. (MVA)	SCP Angle (deg)	L-L, Voltage (kv)	Filter Ratings (MVAR)
4.0	0.3059	180.16	0.0139	5.261	85	3620	85	138	200

Rated active power = 810 MW
Current in the dc system = 1.8 KA
Length of dc transmission line = 895 km

The detailed representation of the ac system at the inverter/rectifier bus is shown in Figure 6. The ac system impedance (component values are shown in Table 1) at the rectifier and the inverter is adjusted to provide short circuit ratios of 4.0 (rectifier) and 1.5 (inverter) with 138 kV at the rectifier ac bus and 230 KV at the inverter bus. These short circuit ratios are chosen to study the influence of low short circuit ratio of the receiving ac system on the system recovery from different faults for various control schemes. Further, each converter at the rectifier and the inverter terminal consists of :

(I) Three series connected six-pulse valve groups per pole, each rated at 150 kV, 1.8 kA.
(II) Converter transformer with leakage reactance of 13% at its own base.
(III) Smoothing reactor of 0.75 H.
(IV) DC filters tuned to 6th and 12th harmonics (component values are shown in Table 2).

Each six-pulse converter at the rectifier and the inverter terminal is simulated using a subroutine. In this subroutine, each valve is individually modelled with an equivalent R-C snubber circuit and phase lock oscillator, which is used to generate firing pulses for each valve[12]. Additionally, the converter transformers are modelled with saturation as shown in Figure 7. The saturation is accounted for by adding an additional flux dependent current to the current computed by the linear part of the model[13]. The V-I characteristics of the transformers are modelled with a knee point voltage of 1.2 p.u. and with an air core reactance double that of the leakage reactance.

The 895 km long dc transmission line separating the inverter and the rectifier stations is modelled as frequency dependent, mutually coupled, distributed line with the following parameters.

Line resistance = 0.0155 ohms/km in the steady-state at 5.0 Hz

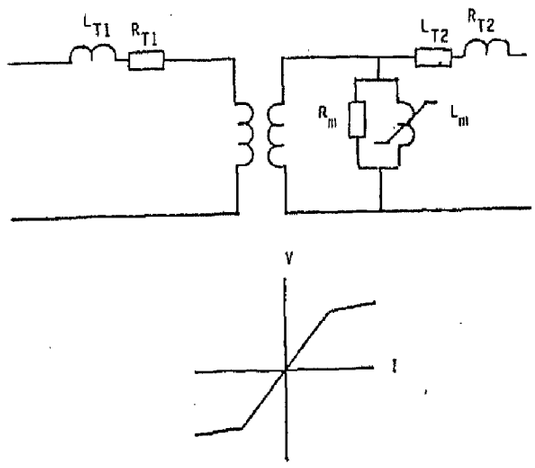


Table 2
DC Filters at the Inverter and Rectifier Terminal

Filter Tuned (Frequency)	Resistance (Ohms)	Inductance (Henry)	Capacitance (μf)
6th	24.0	0.2444	0.80
12th	12.0	0.1222	0.40

Smoothing Reactor Inductance = 0.75 Henry.
Smoothing Reactor Resistance = 1.0 Ohms.

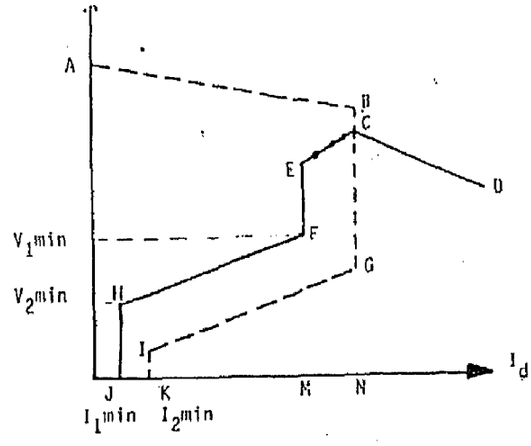
FIG. 7. The converter transformer model.

= 0.019 ohms/km in the steady-state at 90.0 Hz

Mode traveling time = 3.037 ms

Characteristic impedance = 300.00 ohms

The ac system feeding the converter bus at both ends is modelled as an infinite bus. The ac system impedances are represented by R-RL networks having the same damping at the fundamental and the second harmonic frequency. AC filters comprised of the 5th, 7th, 11th, 13th harmonics and high pass are connected at the converter buses as shown in Figure 8. The filter banks at each converter are divided into two equal sections to enable the switching out of 50% of filters after 6-cycles following the dc block for controlling dynamic overvoltages. The components values for ac filters are listed in Table 3.



A-B: α_{min} Control
C-D: γ_{min} Control

JH, EF & EM: Current control for the inverter
IK, BC & GN: Current control for the rectifier
FH & GI: VDCL

FIG. 8. Control characteristic of the HVDC System.

Table 3(a)
AC Filters Components at the Inverter Bus

Filter Tuned (Frequency)	Resistance (Ohms)	Inductance (Henry)	Capacitance (μf)
5	14.22	0.2986	0.9425
7	14.22	0.1222	0.4810
11	5.32	0.0786	0.7395
13	5.32	0.0786	0.5280
HP	94.80	0.0072	2.2795

Table 3(b)
AC Filters components at the rectifier bus

Filter Tuned (Frequency)	Resistance (Ohms)	Inductance (Henry)	Capacitance (μf)
5	5.37	0.1094	2.5725
7	5.37	0.1094	1.3130
11	3.56	0.0207	2.1570
13	3.56	0.0207	1.544
HP	47.20	0.0026	6.1790

Total MVAR Supplied by Filters = 200 MVAR
Number of each filter = 2

5. DC system controls

The dc system is assumed to be operating in the constant current mode without higher level controls. The rectifier operates on constant current control, whereas the inverter controls the voltage by operating at a constant extinction angle control under steady-state. The pole controller determines the firing angle for the complete hvdc system by maintaining the direct current at a constant level. The firing-angle generated by the pole controller (Figure 9) is compared with the firing angle generated by the valve controller shown in Figure 5. The minimum of the two firing angles is selected to send the signal to the firing circuit.

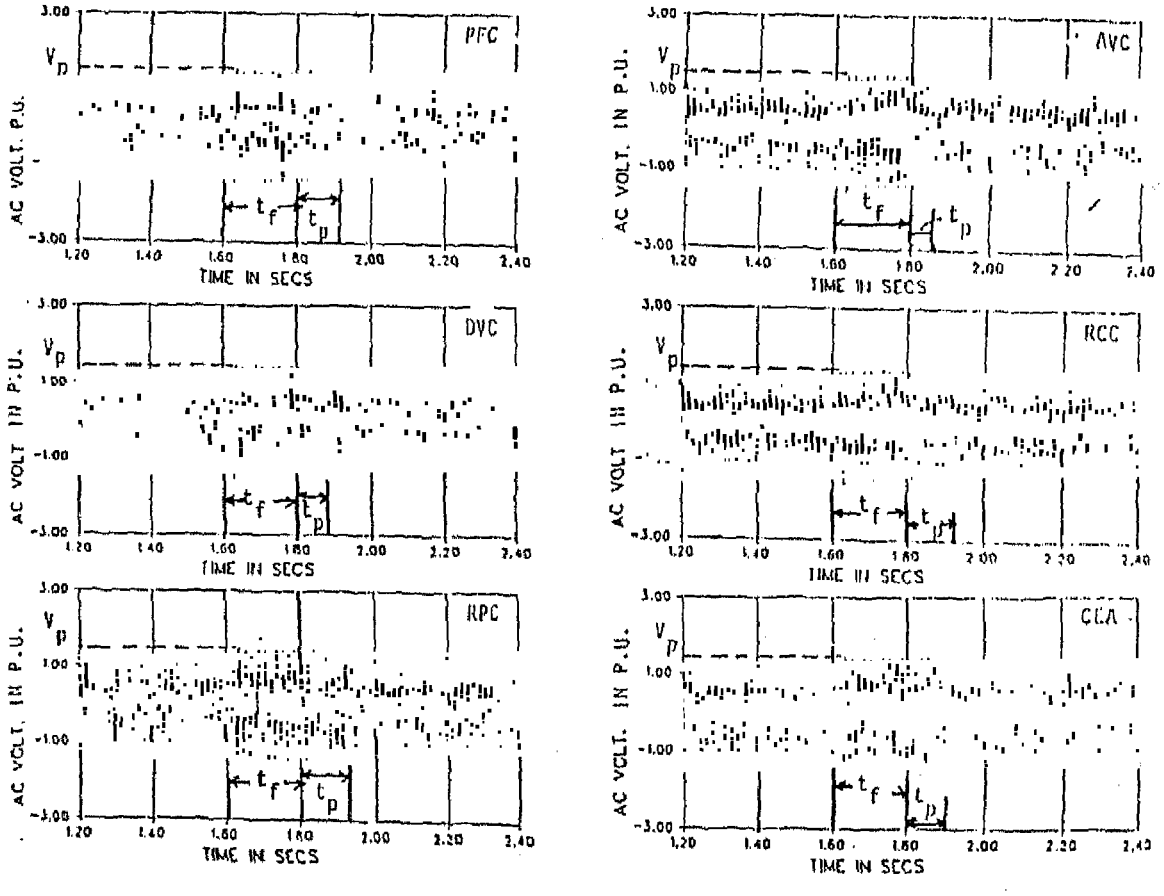


FIG. 9. Instantaneous AC voltage response for the DC line fault at the inverter terminal.

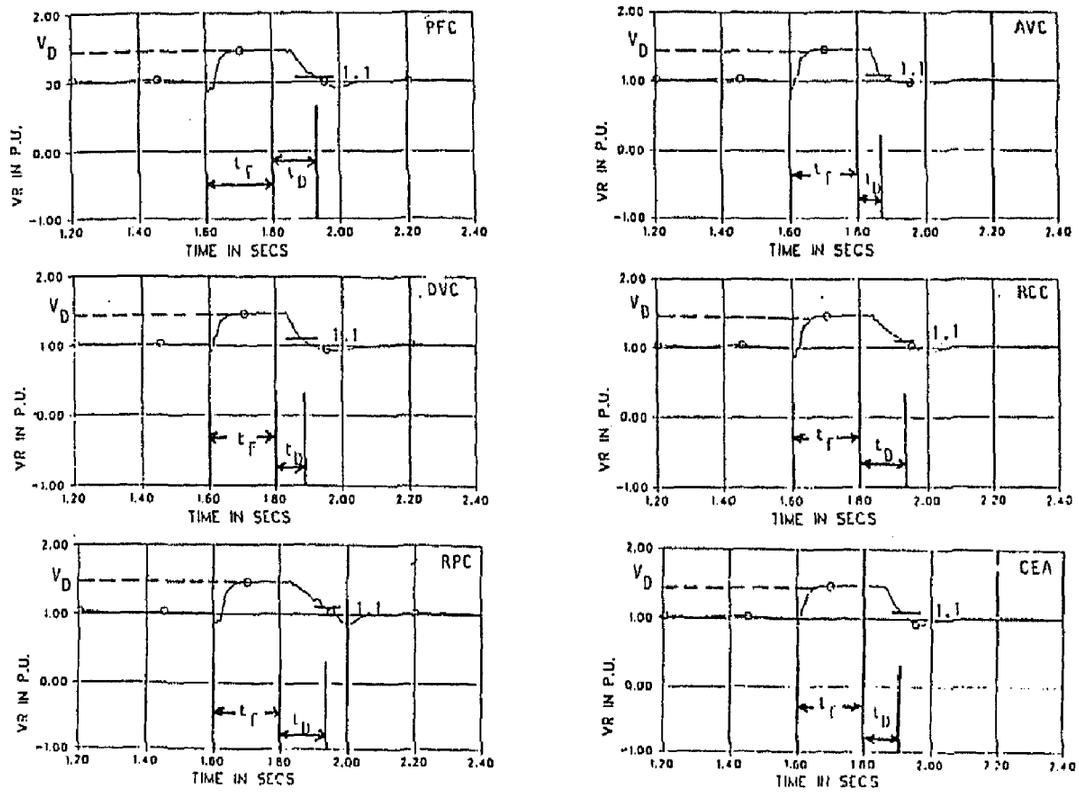


FIG. 10. Three phase RMS voltage response for the DC line fault at the inverter terminal.

The voltage dependent current limit (VDCL) is incorporated to modify the control characteristics as shown in Figure 11 in order to help the system recover from the faults by reducing the direct current order for low operating voltages. If the dc voltage at the rectifier terminal falls below V_{min} for more than 20 msecs, the VDCL is activated, and hence the dc voltage at the rectifier end is limited by the current order to I_{min}. This current order is maintained until dc voltage on the rectifier is less than V_{min}. Once the rectifier voltage is greater than V_{min}, the current order is ramped to 1.0 p.u. The modified control characteristics are shown in Figure 10. The current is ramped from 0.3 to 1.0 p.u. in T_{vdcl} (70 ms).

6. Interfacing of various control modes with EMTDC

The following control modes are realized in FORTRAN programming language.

a) *AC Voltage Control* : The measurement of effective three phase[14] voltage is performed by using a six-pulse diode bridge. The rectified voltage is passed through a low pass, first order filter network to model the delay introduced by the measurement circuit and filters to eliminate the 6th harmonic component of the rectified voltage. This filtered signal is subtracted from the reference signal (1.0 p.u. voltage) to generate the error signal. The error signal is processed by the controller controller to generate the firing angle. The firing angle is limited between 108° and 180°.

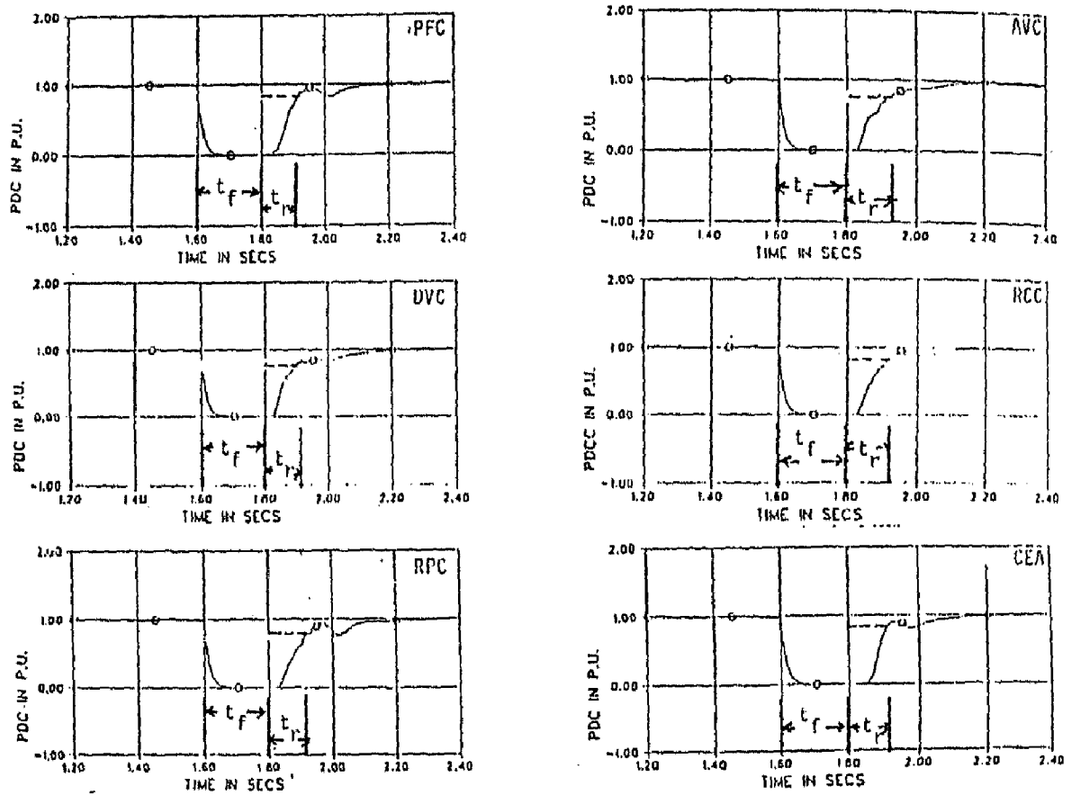


FIG. 11. DC power recovery from DC fault at the inverter terminal.

b) *DC Voltage Control* : The dc voltage is measured before the smoothing reactor at the inverter terminal. The measured signal is passed through a delay circuit to simulate the measurement delay. The delay circuit is realized as follows:

$$\text{Delay Circuit} = \frac{1}{1+T_d s}$$

where T_d = delay in secs;

The measured signal is compared with the reference signal to generate the error signal. The error signal is processed by controller in similar manner as for the ac for the ac voltage control to generate the firing angle.

c) *Power Factor Control* : The power factor at the inverter terminal has been calculated by the following relationship[10] an passed through delay circuits to simulate the measurement delay.

$$\cos\phi = \frac{V_{di}}{K_i V} \tag{22}$$

where $K_i V$ = no load dc voltage

V_{di} = dc voltage at the inverter terminal

During faults, it is possible for "V" to be zero. Hence, equation (1) causes an overflow. This problem has been overcome by setting the power factor at 1.0 for the duration of the disturbance. The error signal is generated by subtracting the measured signal and processing similar to the above-mentioned control schemes. This control is realised without tap changes control.

The power factor control reported in reference[15] is not a real power factor control because it needs assistance from the tap changer control, which makes the power factor response very slow. A pure power factor control is discussed here which does not require the assistance of the tap changer.

d) *Reactive Current Control* : The reactive current at the inverter[16] terminal can be calculated by using equation (2).

$$I_q = K_i I_d \sin\phi \tag{23}$$

where $\sin\phi = \sqrt{1-\cos^2\phi}$

$\cos\phi$ = power factor

I_q = reactive current

This calculated signal is passed through a simple delay circuit to simulate the measurement delay. The firing angle generated by this scheme is similar to that obtained from the a voltage control.

e) *Reactive Power Control*: The reactive power absorbed at the inverter terminal is calculated by using equation (3).

$$Q = VI_q \tag{24}$$

where V = rms voltage for three phase ac voltage

I_q = reactive current

The measurement of "V" is carried out exactly as mentioned for the ac voltage control. The reactive current is calculated by using equation (2). The calculated reactive power is passed through a delay network to simulate the measurement delay. The error is calculated by subtracting measured reactive power from the reference value of the reactive power. The firing angle is generated in a fashion similar to that described for the ac voltage control.

The reactive current control[16] and the reactive power control have some characteristic in steady-state.However, during transients, the as bus voltage is not 1.0 p.u. and the characteristics of the reactive power control become different from the reactive current control. Hence, the investigations are also carried out for the reactive power control.

These measurement schemes are used to realize various control schemes. The effectiveness of various control schemes is evaluated in the next section by investigating system response to some critical faults.

7. Evaluations of HVDC control at the invertor terminal

The suggestion of totally replacing[16] the conventional controls by one of the new control schemes is undesirable because these alternate control modes operate at higher extinction angle,

which results in higher harmonic generation , reactive power demand and losses. Subsequently, the total cost of the station increases.

A better solution[14] is to introduced by new control just after the disturbance for a few cycles to limit over voltages and minimize the possibilities of potential commutation failure. This technique has the merit that during steady state condition the system operate with minimum reactive power demand. In addition the system recovery from fault/disturbance may be improved.

Various views about use of alternate modes at the invertor terminal[14–16] have motivated this steady. The major objective study presented in this paper is to evaluate the effectiveness s of various control schemes at an inverter terminal connected to a weak receiving ac system.

The concept used to evaluate the effectiveness of various control modes is to replace the conventional control by one of the control schemes [*b–e*] for 300 ms just after a fault and then revert it back to the original conventional control. This concept of replacing conventional control by the ac voltage control has been reported in reference[15]. However, this study is limited only to three phase faults at the inverter ac bus. In this paper the effectiveness of the voltage control is studied for many other faults. In addition, to complete the literature, the effectiveness of new control schemes like the dc voltage control, the reactive power control, and the power factor are also investigated.

8. Measures for determining the effectiveness of various control schemes

Comparison of various control schemes has been carried out on the basis of the dc power recovery, peak overvoltages, and dynamic overvoltages.

The three phase to ground fault and the signal phase to ground fault and dc faults are applied, at the inverter end, and three phase to ground fault is applied at the rectifier ac bus also. These faults are assumed to be critical from author's point of view.

9. Controller design for various schemes

The following controller configuration is defined for various control schemes at the inverter terminal of the hvdc system.

$$G_C(S) = K_C\left(\frac{T_C s+1}{s}\right)\frac{(1+T_a s)}{(1+T_b s)} \tag{25}$$

where K_C = controller gain

T_C = controller time constant

T_a, T_b = time constant of the lead-lag network

The controller optimization has also been carried out for the evaluation of the effectiveness of all control schemes. The controller for each control scheme is optimized by observing the system recovery for a given disturbance over a range of controller parameters. The selection of the controller parameters is performed on the basis of the optimum system recovery from the

Table 4
Controller settings for (a) three phase to ground fault at the inverter bus, (b) Single phase to ground fault at the inverter bus, (c) DC line fault, (d) Three phase to ground fault at the inverter AC bus.

(a)					
Name of control scheme	K_P	K_I	T_a	T_b	*Remarks*
PFC	0.60	9.0	0.10	0.02	For conventional control Y_s =
AVC	0.65	18.00	0.06	0.01	0.3, Y_L = 0.5 has been used
DVC	0.20	3.00	0.03	0.01	
RCC	0.30	4.50	0.10	0.02	
RPC	0.250	5.50	0.05	0.01	
(b)					
PFC	0.50	12.00	0.10	0.01	For conventional control Y_s =
AVC	0.45	30.00	0.10	0.03	0.5, Y_L = 0.70.
DVC	0.30	4.50	0.10	0.01	
RCC	0.60	15.00	0.10	0.01	
RPC	0.70	8.50	0.10	0.01	

PFC: Power Factor Control
RCC: Reactive Current Control
AVC: AC Voltage Control
DVC: DC Voltage Control
RPC: Reactive Power Control

(c)					
PFC	0.5	10.5	0.10	0.01	For conventional control
AVC	0.40	40.0	0.10	0.03	Y_s = 0.35 Y_L = 0.55.
DVC	0.35	5.0	0.10	0.01	
RCC	0.80	18.00	0.10	0.03	
RPC	0.85	9.00	0.05	0.02	
(d)					
PFC	0.40	12.00	0.10	0.01	For conventional control
AVC	0.50	38.00	0.07	0.01	Y_s = 0.3330 Y_L = 0.450.
DVC	0.40	7.0	0.10	0.01	
RCC	0.75	16.00	0.10	0.02	
RPC	0.70	11.00	0.10	0.01	

disturbance. The procedure of optimization is repeated for all control schemes for various faults. However, the optimization of various control schemes is valid only for a given system configuration. Once the system configuration changes, the optimization of the controller parameters is to be carried out again for all control schemes for various faults.

10. System response for various faults

The system response for various control schemes is studied by time domain simulation on the EMTDC digital program. The results are summarized below :

Table 5
System response for (a) the three phase to ground fault at the inverter AC Bus, (b) the three phase to ground fault at the inverter AC Bus, (c) the DC line fault at the inverter Terminal, the three phase to ground fault at the rectifier AC Bus.

	Instantaneous Voltage Response		*Dynamic Overvoltage Response*		*DC Power Recovery Time*
Control Scheme	*Highest Magnitude in p.u.* V_p	*Duration in ms* t_p	*Highest Magnitude in p.u.* V_D	*Duration in ms* t_D	t_r *in ms*
(a)					
PFC	2.00	210	1.40	210	210
DVC	2.00	142	1.35	142	210
RPC	1.80	136	1.40	136	210
AVC	2.00	110	1.35	110	210
RCC	1.80	122	1.40	122	210
CEA	2.00	230	1.48	230	210
(b)					
PFC	1.45	71	1.40	71	140
DVC	1.83	80	1.33	80	140
RPC	1.66	122	1.33	122	140
AVC	1.83	52	1.20	52	140
RCC	1.60	135	1.26	135	140
CEA	1.85	135	1.33	135	140
(c)					
PFC	1.5	123	1.5	126	115
DVC	1.5	84	1.5	84	115
RPC	1.5	122	1.5	122	115
AVC	1.5	65	1.5	65	115
RCC	1.5	125	1.5	125	115
CEA	1.5	110	1.5	110	115
(d)					
PFC	1.41	70	1.5	70	132
DVC	1.41	100	1.5	100	132
RPC	1.5	128	1.5	128	132
AVC	1.5	55	1.5	55	132
RCC	1.5	128	1.5	128	132
CEA	1.5	85	1.5	85	132

a) *DC Line Fault* : The duration of this fault is 200 ms. The controller parameters used for system recovery for the fault are listed in Table 4 for various controls.

The investigations are carried out similarly for other faults also. The results for various faults are summarized in Table 5.

11. Discussion

The evaluation of the effectiveness of various control schemes at the inverter terminal of the hvdc system feeding to a relatively weak ac system has been carried out. The effectiv-

various control schemes is determined on the basis of the quality of the system recovery from different ac and dc faults. The quality of the system recovery from different faults is evaluated in terms of the peak instantaneous overvoltages, dynamic overvoltages (magnitude and duration), and dc power recovery time. The concept used for determining the effectiveness of various control schemes is that each control schemes introduced for 300 ms from the instant of the fault and thereafter the inverter operation is reverted to the conventional control. It is found that switching from one control scheme to another without producing significant voltage and power oscillation is possible.

It has been observed that the appropriate choice of controller parameters of all control schemes produces similar ac power recovery time. However, the dynamic overvoltage profile may differ. It has been assumed in the study that the measurement circuit time constant is the same. One can argue that metal oxide arrests can be used to reduce the DOV. However, it clips the peak of DOV only, while control schemes can control the duration of DOV.

12. Conclusions

The evaluation of all control schemes at the inverter terminal of the weak ac system has been performed. The following important conclusions can be drawn :

I. High controller gain lead to instability.

II. Higher short circuit ratio of the receiving ac system improves the stability.

III. Lower short circuit ratio of the sending ac system improves the stability.

IV. The similar dc power recovery time can be obtained by properly choosing the controller parameters for various control schemes.

V. The dynamic overvoltages can be reduced by introducing proper control scheme (Table 5) just after fault for 300 ms and thereafter reverting the system operation to conventional control. This switching in the control schemes provides the advantages of operating the hvdc system with minimum harmonics and reactive power demand steady-state and minimizing DOV during transients.

References

1. Koske, S. and Masada, E., Analytical Design of HVDC Link Control System, *Elect. Engg. in Japan*, Vol. 96, 2, 1976, pp. 80–86.

2. Carroll, D. P., *et al.*, The Use of Voltage Feedback in HVDC Converter Control, *IEEE Trans.*, Vol. PAS-95, 5, 1976, pp. 1579–1589.

3. Yoshida, Y., Development of a calculation method of AC voltage stability in HVDC transmission systems, *Elect. Engg. in Japan*, Vol. 94, 2, 1978, pp. 77–85.

4. Yuki, M., *et al.*, *Development of digitilised control equipment for HVDC transmission, IEEE Trans.*, Vol. PAS 103, Jan. 1984, pp. 190–196.

5. Goudic, D. B., Steady state stability of parallel HV AC-DC power transmission systems, *Proc. IEE*, Vol. 110, 2, 1972, pp. 217–228.

6. Sucena Paiva, J. P., Hernandez, R. and Frerris, L. L., Stability study of controlled rectifier using new discrete nodel, *Proc. IEE*, Vol. 119, 1972, pp. 1285–1293.

7. REEVE, J. AND KAPOOR, S. C., Dynamic fault analysis of HVDC systems with AC representation, *IEEE Trans.*, Vol. PAS-91, **2**, 1972, pp. 508–515.

8. REEVE, J. AND CARR, J., Dynamic simulation of HVDC converter control and its application to system studies, *IEEE Trans.*, Vol. PAS-93, **1**, 1974, pp. 295–302.

9. HINGORANI, N. G., KITCHEN, R. H. AND HAY, J. L., Dynamic simulation of HVDC power transmission systems on digital computers, *IEEE Trans.*, Vol. PAS-87, **4**, pp. 909–916.

10. REEVE, J. AND CHEN, S. P., Versatile interactive digital simulator based on EMTP for AC/DC power system transients, Vol. PAS-103, **12**, 1984, pp. 3625–3633.

11. WOODFORD, D. A. GOLE, A. M. AND MENZIES, R. W., Digital simulation of DC links and AC machines, *IEEE Trans.*, Vol. PAS-102, 1983, pp. 1616–1623.

12. WOODFORD, D. A., Validation of digital simulation of DC links, *IEEE Trans.*, Vol. PAS-104, **9**, 1985, pp. 2588–2595.

13. DOMMEL, H. W., Transformer models in simulation of electromagnetic transients, 5th power system computational conference, Cambridge, England, Sept. 1–5, 1975, pp. 1–16.

14. HAMMAD, A., *et al.*, Advanced scheme for voltage control at HVDC terminals, 1985, PICA, San Francisco, California, May 6-10, 1985, pp. 431–438.

15. NISHIMURA, J., *et al.*, Constant power factor control systems for HVDC transmission, *IEEE* Vol. PAS-95., **6**, 1976.

16. SZECHTMAN, M., *et al.*, Unconventional HVDC controls techniques for stabilization of a weak power system, *IEEE* PAS-103, 1984, pp. 2244–2248.