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Improved active harmonic current compensation of power-electronic load using resonant dc link inverter

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Abstract

This paper proposes an active harmonic current compensator based on Resonant DC Link Inverter (RDCLI) for single-phase systems supplying non-linear loads. This compensator is connected in parallel with any non-linear load through a filter inductance. Compensation of the line harmonics is achieved by injecting harmonic currents into the supply lines such that the compensated line current is in phase with, and of the same shape as the input voltage. The compensator is controlled by a zero-hysteresis bang-bang controller. A new method for current initialization for RDCLI is proposed in this paper. A comparison with the hard-switched PWM inverter based compensator on the same platform is presented. The superior features of the proposed compensator over the PWM-based compensator in terms of efficiency, current regulator bandwidth, response time and spectral performance are established.

Key words: *Harmonic compensation, RDCLI.*

Major Discipline: Power Quality.

1. Introduction

The extensive use of industrial loads such as static power supplies and converter-fed drives leads to waveform degradation in power supply networks. This is a matter of serious concern both for the customers and the utility. On the other hand, the demand for clean power in use of sensitive loads such as computers, electronic equipment, and automated processes continues to grow. A number of techniques such as use of passive filters, PWM schemes, active filtering[1–5] hybrid filtering [6] etc. have been suggested in literature for compensation of line harmonics. However, all these schemes suffer from one or more drawbacks such as load dependence, large system size, poor system efficiency, and complexity of control.

Out of the several schemes suggested in literature, the PWM shunt compensator is most widely used. However, this compensator has its inherent limitations of high switching losses because of hard switching. This puts a constraint on the maximum switching frequency. It also requires a large dc link filter. The problems like acoustic noise and EMI due to large di/dt and dv/dt are common in a PWM system. For proper current tracking the approximate current bandwidth is usually the PWM frequency divided by a factor of ten. Therefore, PWM based compensator fails to track high frequency components particularly at high power level. For example, if the harmonics up to nineteenth are to be considered for a 500 kW converter load then the compensator should have a power rating of 100 kVA and it must be capable of switching at

a frequency of about 9.5 kHz or higher. This is a difficult task given the present status of power semiconductor device technology. Without adequate current regulator bandwidth, compensation can never be perfect as there will be phase shift error and chattering in the compensated current drawn from the source. The hard-switched PWM inverter based active compensator does not have a rapid response as desired. There is a minimum delay time of 4 ms (1/4th of a cycle in a 60 Hz system) while tracking a current in response to load change as reported in literature[7].

For active harmonic current compensation (or active filtering), a high power topology with adequate current regulator bandwidth is necessary. In addition, the response time should be fast. In essence, we must be able to realize a large capacity non-sinusoidal current source generator which must follow its command instantaneously[8].

Keeping in view of the above considerations this paper presents an active harmonic current compensator which uses a resonant dc link inverter (RDCLI) as power circuit and is connected in parallel with a power-electronic load. Compensation is achieved by injecting an instantaneous current into the supply lines to cancel the harmonics. This compensator can achieve high efficiency by reducing switching losses. This topology also offers adequate current regulator bandwidth for compensating higher order harmonics because of high frequency switching. Moreover, the transient response is fast and the control is simple.

2. RDCLI Topology

The RDCLI was first proposed by Divan[9]. This soft-switched converter is suitable for high power applications (Up to 500 kVA).This topology is same as that of a PWM VSI circuit except that an inductor and a capacitor are added in the link for resonance. The link voltage goes through periodic zero crossings during which switching transitions are carried out. Fig. 1 shows the equivalent circuit of an RDCLI. I_0 represents current drawn by the inverter (switching network) which is actually the load current of the inverter. The IGBT shown in Fig. 1 represents the switch across the link. The RDCLI topology offers the following advantages:

- The switching loss is practically zero because of zero voltage switching (ZVS).
- The frequency of operation is very high.
- Snubber circuits are not required.
- Reliability is higher from the heat sink point of view.
- EMI is less and acoustic noise is not present.
- Fast transient response.

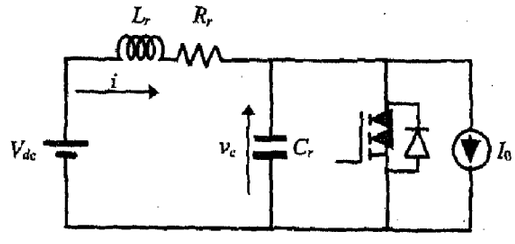

FIG. 1. Equivalent circuit of RDCLI.

This topology offers adequate current regulator bandwidth because of high frequency operation. However, this circuit is sensitive to initial current in the inductor. Zero crossing failure may occur if current initialization is not done properly. The other major problem is that the voltage stresses across the devices are large. Usually clamping circuits are used to reduce voltage stresses.

3. Active harmonic current compensation principle

The block diagram of the compensating scheme is shown in Fig. 2 in which a single-phase ac source is supplying a rectifier (or any other non-linear) load. In the absence of a compensator, the source current is nonsinusoidal, comprising of fundamental and harmonics that might affect the other loads connected to the ac bus. If the harmonic components are compensated, then the source current becomes sinusoidal. The compensation is achieved on the basis of instantaneous current injection.

To compensate for the harmonic current an RDCLI is connected in shunt at the load terminals as shown in Fig. 2. Let i_L and i_S be the current drawn by the load from the source and the desired source current, respectively. For ideal compensation, the source should supply only the active part of the fundamental component of the load current and the compensator should supply the reactive fundamental component and all harmonic components. For a specific load current and converter topology, it is possible to determine the desired source current for perfect compensation. Thus i_S is taken to be equal to the magnitude of the active part of the fundamental component of i_L. Then the current that must be supplied by the active harmonic current compensator (AHCC) can be obtained by applying Kirchoff's current law at the shunt point as $i_H = i_L - i_S$. The AHCC is then switched in such a way that the instantaneous current through the inductor L_F follows i_H.

4. Proposed AHCC

As mentioned above, the basic philosophy of an AHCC is to generate a nonsinusoidal current following a command. The RDCLI based AHCC control comprises of two parts - (1) choosing

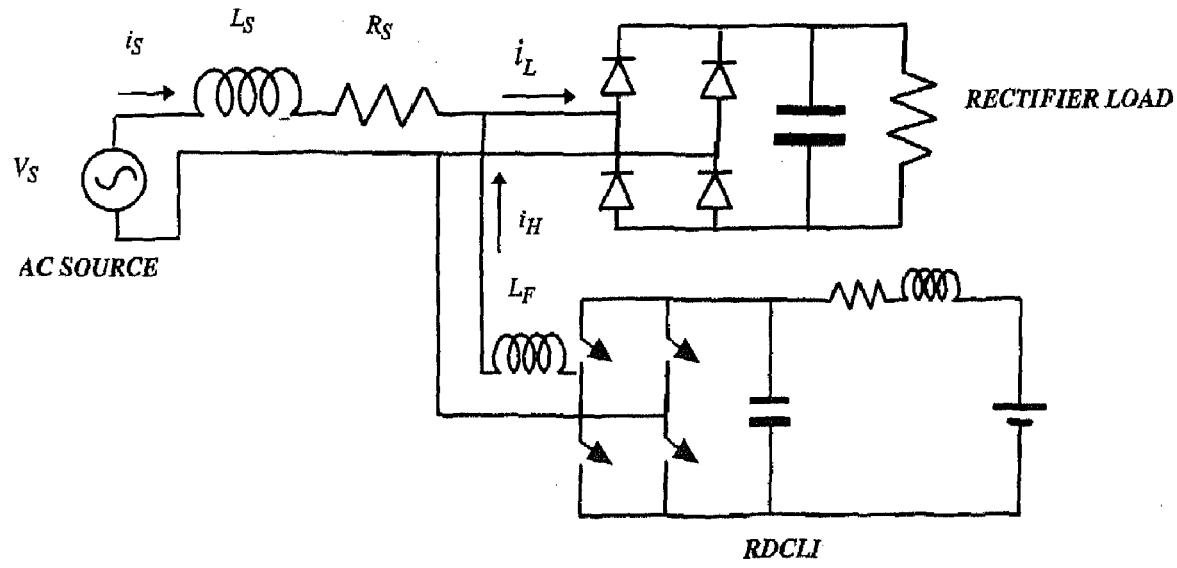

FIG. 2. Schematic diagram of the current compensating scheme.

a proper value of initial current to avoid zero crossing failure in RDCLI and (2) current tracking. These are discussed below.

4.1. *Proposed Current Initialization Technique*

Lai and Bose[10] pointed out that the value of the current in the inductor L_r (refer Fig. 1) at the beginning of the resonant cycle is critical to ensure that no zero crossing failure occurs in the circuit. Consider for example Fig. 3 in which the voltage across the capacitor C_r and the current through the inductor L_r are shown. Starting at the instant t_0, the capacitor reaches zero voltage at instant t_1. The switching of the devices in the inverter circuit is performed during this zero voltage state to minimize switching losses. The inductor current increases almost linearly during this period t_2–t_1. The instant t_2 is so chosen that the current at this instant is sufficient to bring the capacitor voltage zero again after a resonant cycle.

In this paper we propose a scheme in which the duration $t_3 - t_2$ is fixed at ΔT microseconds. It is to be noted that the particular value of ΔT chosen depends on the parameters of the resonant circuit. The state space equation of the resonant circuit shown in Fig. 1 is given by

$$\dot{x} = Ax + Bu \tag{1}$$

where $x = \begin{bmatrix} v_c & i \end{bmatrix}^T$, $u = \begin{bmatrix} I_0 & V_{dc} \end{bmatrix}^T$ and

$$A = \begin{bmatrix} 0 & 1/C_r \\ -1/L_r & -R_r/L_r \end{bmatrix}, \quad B = \begin{bmatrix} -1/C_r & 0 \\ 0 & 1/L_r \end{bmatrix}$$

The solution of the above equation at instant t_3, based on the initial conditions at instant t_2 is

$$x(t_3) = e^{A\Delta T} x(t_2) + \int_0^{\Delta T} e^{A(\Delta T - \tau)} Bu(\tau)\, d\tau \tag{2}$$

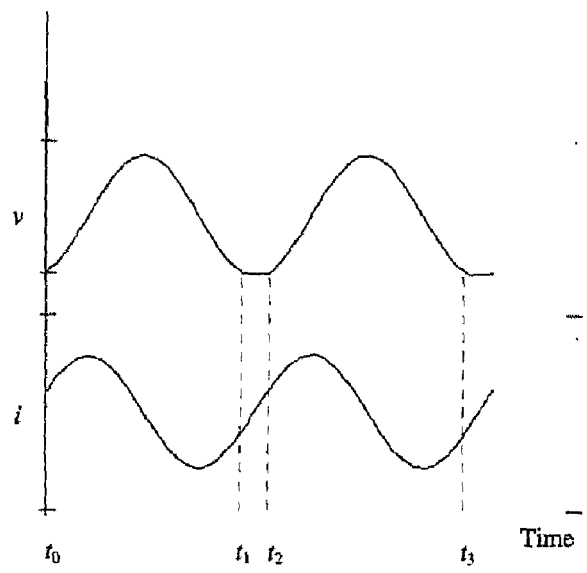

FIG. 3. Link voltage and current waveforms.

It is to be noted that in the above equation V_{dc} is constant and $I_0(t_2)$ is assumed to be known. Also noting that capacitor voltage must be equal to zero at instant t_3, defining a row vector C as $C = [1\ 0]$ we can write from (2)

$$0 = C[\phi x(t_2) + \theta u(t_2)] \tag{3}$$

where $\phi = e^{AT}$ and $\theta = \int_0^{\Delta T} e^{A(\Delta T - \tau)} B d\tau$. Note that the above equation is obtained by assuming that I_0 remains constant between t_2 and t_3. This is a valid assumption as this current is flowing through the inductor L_F (see Fig. 2) which is much larger than L_r. Again in (3) the initial condition is $x^T(t_2) = [0\ i(t_2)]$ Thus the value of the current i at instant t_2 required to ensure zero crossing of the voltage at instant t_3 can be computed from (3).

Once $i(t_2)$ is obtained the time for which the capacitor should be shorted is calculated as follows. The circuit equation for the time interval between t_1 and t_2 is given by

$$\frac{di}{dt} = -\frac{R_r}{L_r} i + \frac{1}{L_r} V_{dc} \tag{4}$$

The solution of the equation is given by

$$i(t_2) = e^{-(R_r/L_r)\Delta t} i(t_1) + \int_0^{\Delta t} e^{-(R_r/L_r)(\Delta t - \tau)} V_{dc} d\tau \tag{5}$$

where $\Delta t = t_2 - t_1$. Equation (5) is solved to obtain an expression for Δt as

$$\Delta t = \frac{L_r}{R_r} \ln\left\{\frac{i(t_1) - V_{dc}/R_r}{i(t_2) - V_{dc}/R_r}\right\} \tag{6}$$

4.2. *Current tracking*

A zero-hysteresis bang-bang control is used for current control. However, in this system, the switching transitions takes place only at the prescribed instants when the link voltage is zero.

The actual output current of the inverter is compared with the reference (command current, i_H in Fig. 2) current. Based on the error signal a switching decision is taken such that the inverter output voltage is SV_{link} where S may have values 1, 0 or -1 so that the current regulator makes the current as close to its command i_H as possible[11].

5. Simulation results

The RDCLI active harmonic current compensator is simulated using the MATLAB software package. All the simulations are carried out for a single phase system. The system parameters chosen are:

$$V_{dc} = 385\,V, \quad L_F = 15\,mH, \quad R_F = 0.2256\,\Omega, \quad v_s = 440\sqrt{2/3}\sin(100\pi t)\,V$$
$$L_r = 63.32\,\mu H, \quad C_r = 1\,\mu F, \quad R_r = 0.0531\,\Omega$$

It is also assumed that $L_S = R_S = 0$. The link frequency chosen is 20 kHz. Ideally, the load should draw only the in phase fundamental component of the load current. In our simulation it is assumed that magnitude of i_S is equal to the fundamental component of i_L and it is in phase with the supply voltage.

The current regulator bandwidth of a RDCLI compensator is tested by subjecting the compensator to track frequency components from 50 Hz to 1150 Hz. Some sample results are shown in Figs. 4 and 5 which show compensated current and the reference current from the source when the compensator tracks 13th (650 Hz) and 23rd harmonic (1150 Hz) components respectively. The command current for the compensator and the actual current from the compensator for these cases are also shown. The compensator tracks all these components faithfully without any phase shift error. This clearly implies that since RDCLI can fabricate these frequency components, RDCLI based AHCC can compensate both lower as well as higher order harmonics in the load. The compensated current from the source becomes smoother as the link switching frequency increases. The simulations are carried out at three different link frequencies, 20 kHz, 40 kHz and 80 kHz. ΔT chosen for the above three frequencies are 45 μs, 22.5 μs and 11.25 μs respectively. It is assumed that the non-linear load draws a current which contains 3rd, 5th, 7th, 9th, 13th, 23rd harmonics in addition to the fundamental. The magnitude of the harmonic components with respect to the fundamental are inversely proportional to the harmonic number. Note that this particular choice of the load current is to demonstrate the performance of the AHCC and not based on any particular power-electronic load. The compensated source current for these frequencies is shown in Fig. 6. It is seen that even though compensated current becomes smoother with an increase in the link frequency, the notches that are visible around the peak of the current waveform only get reduced but not eliminated.

These notches can be reduced significantly by increasing the dc source voltage V_{dc}.. As the phase of the source current coincides with that of the source voltage the voltage difference be

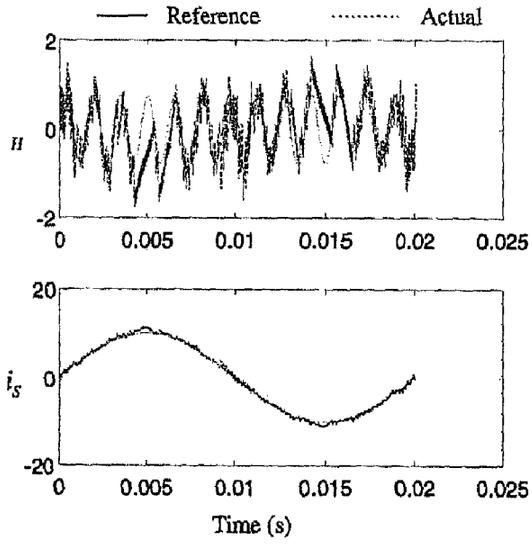

FIG. 4. Compensator current and compensated current from source in the presence of 13th harmonic.

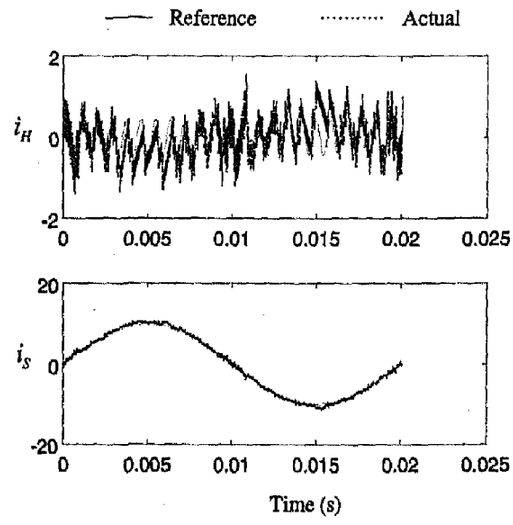

FIG. 5. Compensator current and compensated current from source in the presence of 23rd harmonic.

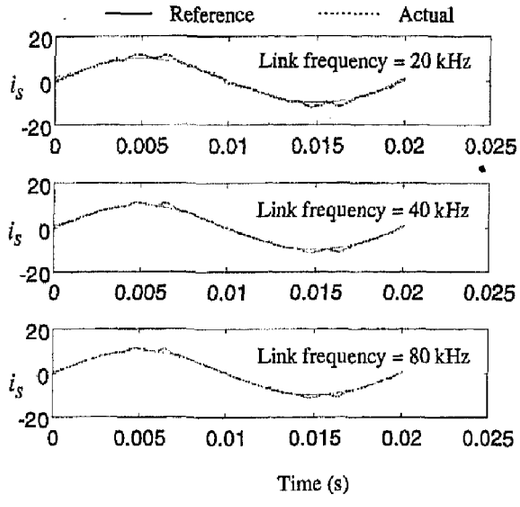

FIG. 6. Effect of link frequency variation on compensation.

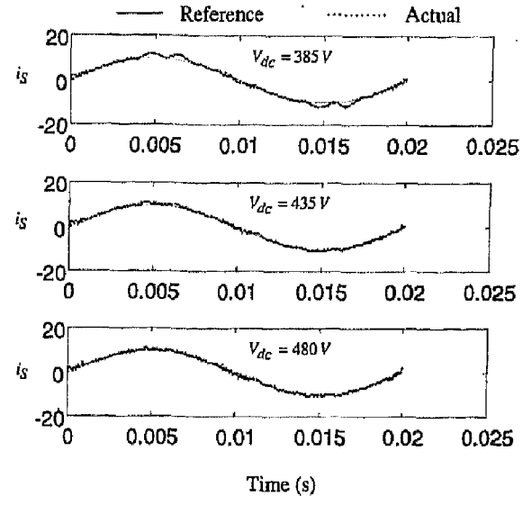

FIG. 7. Effect of dc source voltage variation on compensation.

tween the inverter and the source is minimum during the period when these notches are present. Thus to force a current rapidly (to track fast changing command) through a large inductor L_F this higher level of dc voltage is necessary. Fig. 7 shows compensated currents and the reference currents from the source at three different values of dc source voltages, i.e. 385 V, 435 V and 480 V. These simulations are carried out at a link switching frequency 20 kHz. The notches present in Fig. 6 now disappear with an increase in the dc source voltage. However there seems to be slight increase in chattering in the compensated current waveform in the other regions of the sinusoidal waveform. This is explained by considering the fact that the rate of rise of current through the filter inductor increases as the value of V_{dc} becomes higher.

Having studied the effects of dc bus voltage variation and link frequency variation on the performance of compensator, a case study has been taken up when the compensator supports a typical non-linear load. In this simulation dc bus voltage chosen as 470 Volts and the link frequency chosen is 40 kHz. The load is assumed to draw current from the supply source which contains harmonics 3rd, 5th, 7th, 9th, 13th and 23rd in addition to the fundamental. It is to be seen how the compensator performs with the parameters chosen earlier. Fig. 8 shows the compensated current from the source and the reference current. From this figure it can be inferred that RDCLI AHCC compensates all the harmonics. The ripples in the compensated current is minimum and there is no phase shift error.

The performance of the compensator can be judged by its ability to reduce the harmonic components of the supply current to a minimum. Fig. 9 shows the spectral response of the uncompensated system and the compensated system. It is observed that RDCLI compensator compensates all the harmonics and reduces all these components at least by 40 dB. The total harmonic distortion in the absence of the compensator is 43.78% in the current drawn from the source. The THD reduces to 2.24% after compensation. The requirements specified by the utilities usually are that the THD should be below 5% and any single frequency component should be below 3% of the fundamental. Both the above conditions are satisfied by the pro-

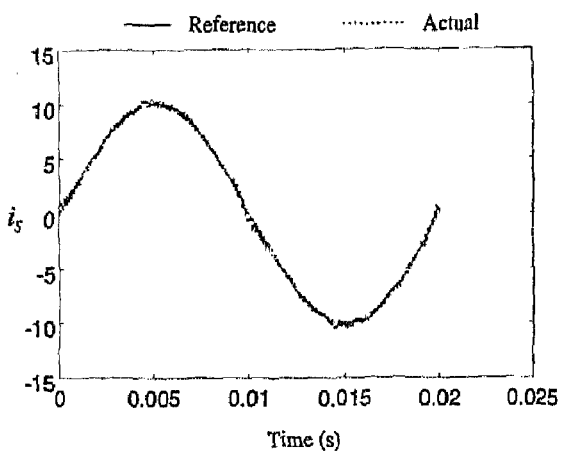

FIG. 8. Compensator performance for V_{dc} of 470 V and link frequency of 40 kHz.

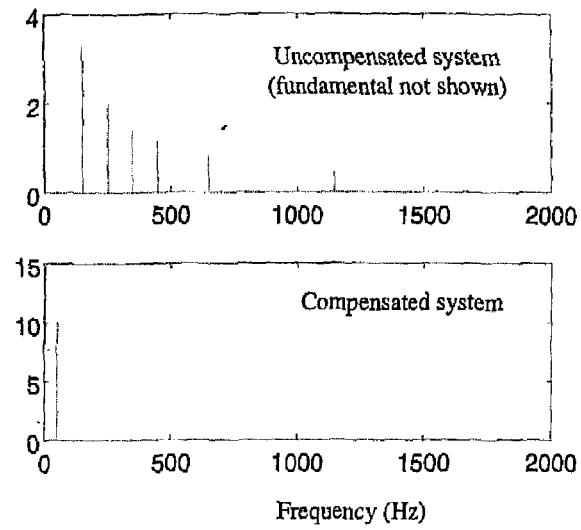

FIG. 9. Spectral performance of the compensator for V_{dc} of 470 V and link frequency of 40 kHz.

AHCC. The THD in the compensated source current is usually treated as a figure of merit for any compensator and in this regard the compensator performance can be considered to be excellent.

Moreover, this compensator adapts to load change almost instantaneously. Fig. 10 shows the compensator response when the load current is increased by 100% after a cycle. It can be seen that compensator tracks the changed current almost instantaneously. Following the detection of a change in the load current, a change in the switching decisions has to be taken as the command for the compensator changes. The AHCC performs the required switchings to track the new command current. However there is a delay of one resonant cycle before the compensator begins to act. This is negligibly small.

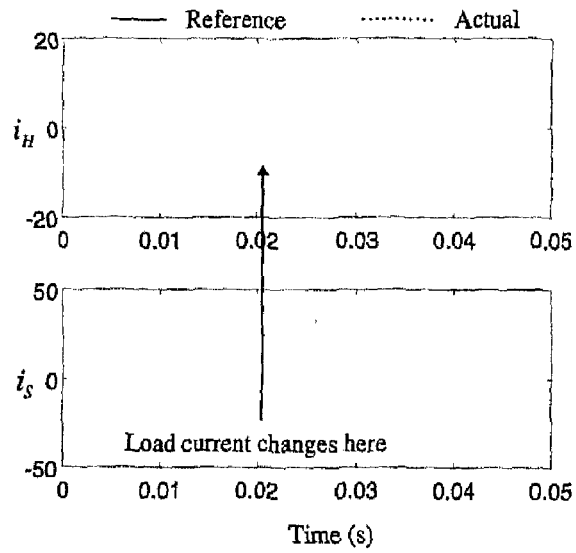

FIG. 10. Transient response of the compensator when the load current is doubled.

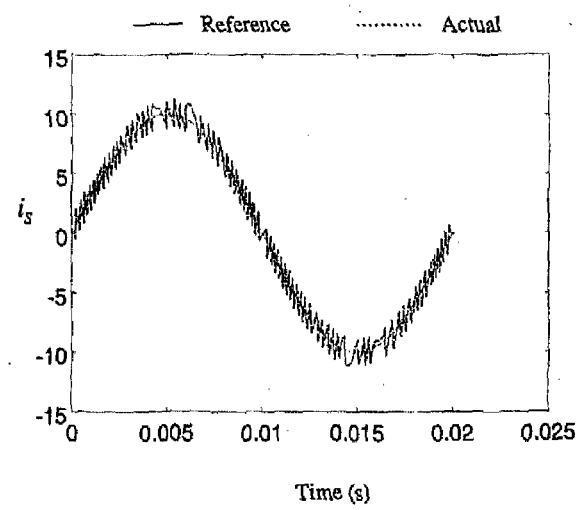

FIG. 11. Reference current and compensated current from source for a PWM inverter based compensator working at $V_{dc} = 470$ V and average switching frequency of 8 kHz.

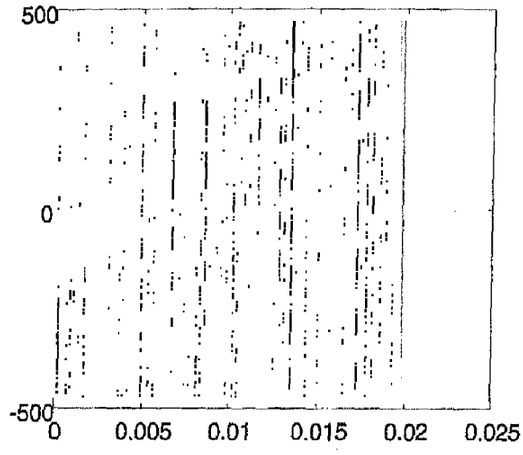

FIG. 12. PWM inverter voltage waveform for the case of Fig. 11.

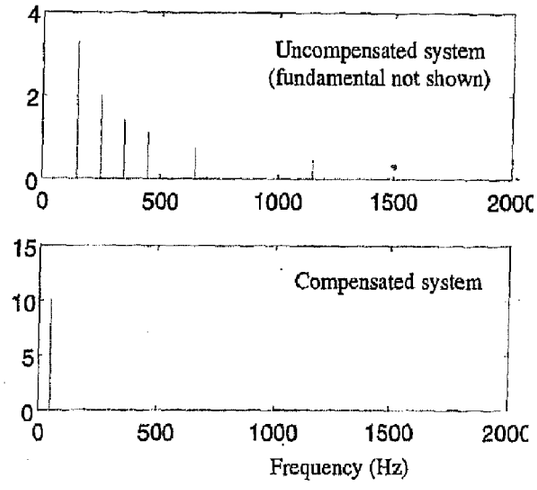

FIG. 13. Spectral performance for PWM inverter based AHCC.

6. Comparison with hard-Switched PWM inverter based AHCC

A conventional hard-switched PWM VSI is used as power circuit. In order to bring out a comparison with the proposed compensator in the same platform this PWM inverter based AHCC is also allowed to support the same non-linear load as before. The conventional hysteresis band control is used for current control in the inverter. The hysteresis band is fixed to 10% of the peak value of the reference current. The switching instants are defined as in a standard hysteresis regulator, i.e., the switching takes place when the absolute value of current error equals to h (hysteresis band). The parameters used for simulation are the same as before.

Fig. 11 shows the reference current and the compensated current from the source. There is a reasonable amount of chattering in the compensated waveform. Moreover the phase error is significant. Fig. 12 shows the inverter output voltage. The average switching frequency of the inverter is now 8 kHz. The chattering and the phase shift error seen in Fig. 11 can be reduced further by decreasing the hysteresis band h. However, this will effectively increase the switching frequency of the PWM inverter. Even it is difficult to operate a hard-switched PWM inverter at a switching frequency of 8 kHz when the power level is about 100 kW or more. Fig. 13 shows the spectral response of the uncompensated current and the compensated current from the source. THD in this case reduces to 3.63% after compensation. Four of the single frequency components i.e., 2nd, 3rd, 5th and 7th harmonics are about 3% of the fundamental. The restrictions imposed by the utilities can be overcome by increasing the switching frequency, but that will increase the switching losses considerably.

From the above simulation studies we can bring out the comparative merits of a soft-switched RDCLI based AHCC over a hard-switched PWM inverter based AHCC. A comparative figure of merit vis-à-vis the total harmonic distortion (THD) for the two different compensators discussed above is given in Table 1.

- The switching losses are negligible in RDCLI based AHCC because of ZVS.

Table 1
THD of the two compensators

Type of Compensator	*% THD*
PWM based AHCC operating at 2 kHZ	7.83
PWM based AHCC operating at 8 kHZ	3.63
RDCLI based AHCC operating at 40 kHZ	2.24

- The proposed AHCC is capable of compensating lower as well as higher order harmonics at a reasonably high power level where a PWM inverter based compensator finds limitations because of inadequate current regulator bandwidth.
- RDCLI based AHCC has a fast transient response following its command almost instantaneously. This is extremely fast compared to its PWM counterpart.
- Superior Spectral Performance.

7. Conclusions

The study of Resonant DC Link Inverter as an active harmonic current compensator reveals that it is possible to compensate the harmonic currents generated in the source by the non-linear loads. The simulations indicate that THD and different individual harmonics in the compensated current are well below the limits prescribed by the power utilities. A judicious choice of the level of link voltage and the switching frequency of the inverter makes the compensator perform better. The compensator is shown to provide fast response to changing load conditions. The compensator can be designed for high power level depending upon the availability of fast switching high voltage and high current devices such as IGBT's. A comparison with hard-switched PWM inverter- based AHCC establishes the superior features of the proposed compensator in terms of efficiency, fast transient response, current regulator bandwidth and spectral performance.

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