

A constant frequency resonant transition converter

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Abstract

High power densities can be achieved in switched-mode power supplies, by switching at very high frequencies. The resonant transition converters have many desirable features at such high frequencies. One such converter, namely, the phase-modulated full-bridge converter (PMC) is presented in this paper. The basic principles of operation are briefly discussed. The various trade-offs involved in the design are explained. Experimental and simulation results, obtained on a 560 W/250 kHz PMC, with a power density of nearly 5 W/inch³ (0.3 W/cm³), are presented.

Keywords: High-frequency switched-mode power supplies, resonant converters, zero-voltage switching, phase modulation.

1. Introduction

The increasing demand for higher power densities in switched-mode power supplies is pushing the switching frequencies into the MHz region. Since the size of the power transformer and the energy storage elements are a strong function of the switching frequency, significant savings in size and weight are possible with such high frequencies. However, with conventional PWM topologies, the switching losses also increase proportionately with the frequency of operation. The larger heatsinks thus required totally offset the above-mentioned savings. In order to realise the high power densities possible with high switching frequencies, it is therefore essential to reduce the switching losses.

Resonant load converters¹ and resonant switch converters² with either zero-current switching (ZCS) or zero-voltage switching (ZVS) have been proposed to address these problems. In these converters the switch current or the voltage is made sinusoidal by adding an extra resonating LC tank circuit. In ZCS, the device is switched off at the zero-crossing of the sinusoidal current and in ZVS, it is turned on when the sinusoidal voltage across it reaches zero. Thus the switching losses are greatly reduced in these converters. However, they have the following two serious drawbacks:

- device voltage/current stress is much larger, typically 3 to 4 times that of the corresponding PWM topologies. The conduction losses are hence much larger.
- output control is by varying the operating frequency. The output filters, therefore, have to be designed for the lowest frequency and hence are not optimally utilised.

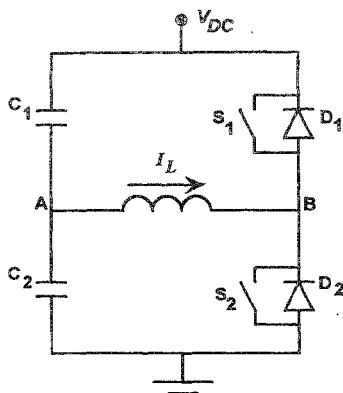


FIG. 1. Half-bridge converter.

Resonant transition converters², being proposed recently, combine the low switching loss characteristics of the resonant converters and the low conduction loss and constant frequency characteristics of the PWM converters. The phase-modulated full-bridge converter, presented in this paper, belongs to this class of converters and offers ZVS characteristics. Except for the resonant transitions, it is identical to the square-wave PWM full-bridge topology. The design principles for the two schemes are hence very similar. ZVS in PMC is obtained relying mainly on the parasitic components like the magnetizing and leakage inductances of the power transformer and the output capacitance of the MOSFET switch. These features make PMC the preferred topology for high-voltage and high-frequency applications.

2. Basic principle of operation

In any double-ended converter, like the push-pull, half-bridge, etc., it is possible to design for zero-voltage switching, if the duty ratio is kept fixed at 50%. This basic principle may be brought out by considering the half-bridge converter shown in Fig. 1. Consider S_2 conducting initially, resulting in the current I_L . As S_2 is switched off, the inductive nature of the load forces I_L to continue to flow in the same direction, but now completing the path through D_1 and C_1 . Since D_1 is conducting, the voltage across the switch S_1 is zero. Hence, turning on S_1 now results in ZVS. The duration for which D_1 conducts depends on the nature of the load and the energy stored in it. Hence to reliably turn on S_1 with zero volts across it, it is necessary that it is switched on after S_2 is switched off and while D_1 is conducting. Similarly, S_2 should be turned on after S_1 is turned off and D_2 is conducting. In a symmetrical half-bridge converter, this implies operating with the fixed duty ratio of 50%.

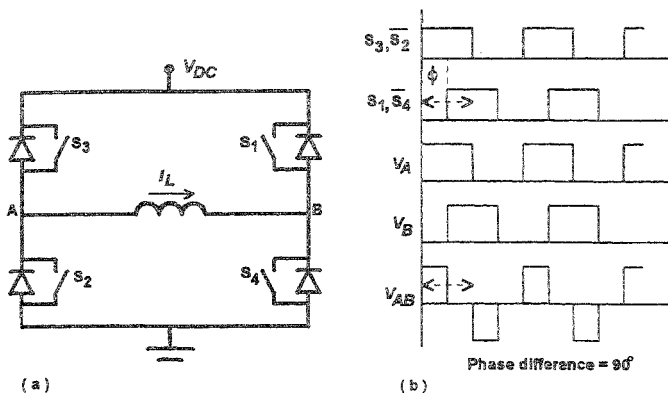


FIG. 2. Phase-modulated converter. a. simplified schematic, and b. waveforms for 90° phase difference.

With the duty ratio fixed at 50%, output regulation is not possible. Therefore, alternative methods have to be employed to achieve regulation. For the full-bridge topology, phase modulation, explained with the help of Fig. 2, is one such alternative.

Figure 2a shows the simplified schematic of the phase-modulated full-bridge converter. Each of the four devices (S_1 to S_4) is operated at 50% duty ratio. Hence the waveforms at points A and B are square waves with 50% duty ratio as shown. Phase modulation simply refers to varying the phase difference between these two square waves, to achieve output control. Phase difference of 180° corresponds to the maximum output voltage. As the phase difference is reduced, the output reduces proportionately. Figure 2b shows the output for a phase difference of 90° . The sequence of operation in a complete cycle is explained in the next section.

3. Analysis of a complete cycle of operation

Figure 3 shows the schematic of PMC used for analysis and simulation. As may be seen the figure includes the parasitic elements like the output capacitance (C_1 , C_2 , C_3 and C_4) of the MOSFET and the magnetizing (L_m) and leakage (L_{lk}) inductances of the transformer. Zero voltage switching demands that, before a MOSFET is switched on, its output capacitance be completely discharged. This discharge is accomplished by the energy stored in the magnetizing and leakage inductances. Therefore, these parameters are crucial from the ZVS viewpoint and have to be considered in the analysis.

For the purpose of analysis, a complete cycle of operation is divided into eight distinct intervals for the inverter and four intervals for the secondary side rectifiers. The

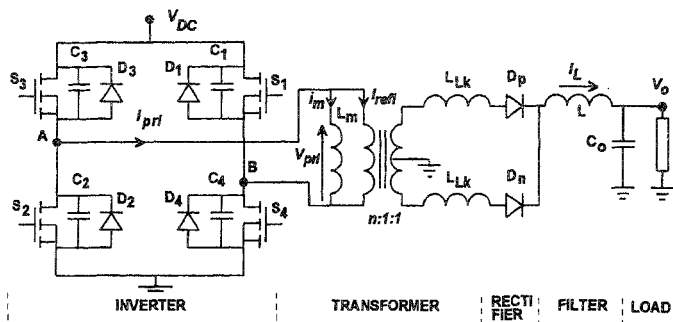


FIG. 3. Schematic diagram of the PMC.

inverter and rectifier intervals are interdependent. The transformer primary currents are determined by the secondary side diode currents which in turn depend on the magnitude and polarity of the inverter voltages. However, for ease of analysis they are considered

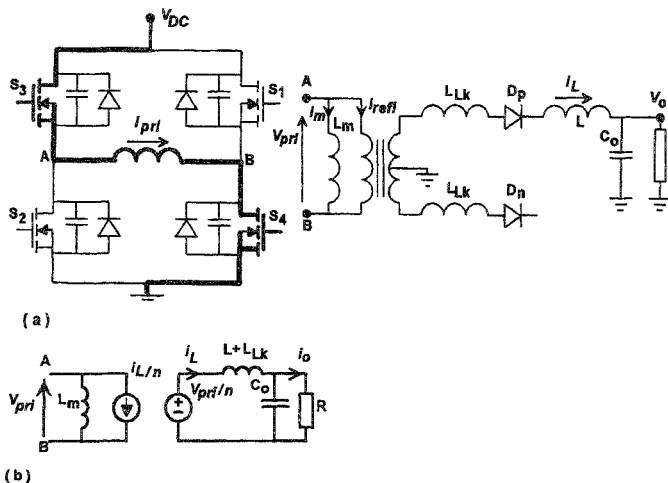


FIG. 4. PMC in inverter interval I. a. devices conducting, and b. equivalent circuit.

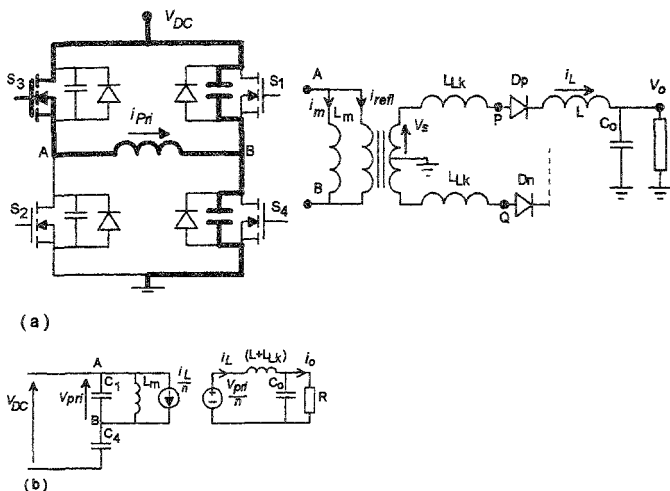


FIG. 5. PMC in inverter interval 2. a. devices conducting, and b. equivalent circuit.

separately. The inverter intervals are determined by the switching sequence of the devices. Figure 4 shows the inverter in interval 1, highlighting the devices conducting, and the current path. During this interval the diagonal switches S_3 and S_4 conduct, transferring power to the load. This interval ends when S_4 is switched off. The governing equations for the inverter are

$$L_m \cdot \frac{d}{dt} i_m = V_{pri} \quad (1)$$

$$i_{pri} = (i_m + i_{refl}) \quad (2)$$

$$i_{refl} = (i_{Dp} - i_{Dn})/n. \quad (3)$$

The above three equations are general and are valid in all the intervals. The equations valid in interval 1 alone are,

$$V_{C_1} = V_{C_2} = V_{DC} \quad (4)$$

$$V_{C_3} = V_{C_4} = 0 \quad (5)$$

$$V_{pri} = V_{DC}. \quad (6)$$

Table I
Sequence and governing equations of the inverter intervals

U	Devices on	From	To	V _{C1}	V _{C2}	V _{C3}	V _{C4}	V _{pn}
1	S ₃ S ₄	S ₃ on	S ₄ off	V _{DC}	V _{DC}	0	0	V _{DC}
2	S ₃ C ₄ C ₁	S ₄ off	S ₁ on	V _{DC} - V _{C4}	V _{DC}	0	$\frac{dV}{dt} = \frac{-i_{pn}}{2C}$	V _{C1}
3	S ₂ D ₁	S ₁ on	S ₃ off	0	V _{DC}	0	V _{DC}	0
4	D ₁ C ₃ C ₂	S ₃ off	S ₂ on	0	V _{DC} - V _{C3}	$\frac{dV}{dt} = \frac{-i_{pn}}{2C}$	V _{DC}	-V _{C3}
5	S ₁ S ₂	S ₂ on	S ₁ off	0	0	V _{DC}	V _{DC}	-V _{DC}
6	S ₂ C ₁ C ₄	S ₁ off	S ₄ on	$\frac{dV}{dt} = \frac{-i_{pn}}{2C}$	0	V _{DC}	V _{DC} - V _{C1}	-V _{C4}
7	S ₂ D ₄	S ₄ on	S ₂ off	V _{DC}	0	V _{DC}	0	0
8	S ₄ C ₂ C ₃	S ₂ off	S ₃ on	V _{DC}	$\frac{dV}{dt} = \frac{-i_{pn}}{2C}$	V _{DC} - V _{C2}	0	V _{C2}

The second interval starts when S₄ is switched off. The primary current which was initially flowing through S₄, now begins to flow through C₄ and C₁ as shown in Fig. 5. From the equivalent circuit shown in Fig. 5b, the governing equations valid for this interval can be derived as

$$\frac{d}{dt} V_{C4} = \frac{i_{pn}}{2C}; (C = C_1 = C_2 = C_3 = C_4), \quad (7)$$

$$V_{pri} = V_{C1} = (V_{DC} - V_{C4}). \quad (8)$$

Interval 2 ends when S₁ is switched on. The equivalent circuit for the other inverter intervals can be established by similar analysis and the corresponding equations derived⁴. Table I lists the start and end of each interval, and the equations valid in them.

The rectifier intervals are determined mainly by the transformer voltages. In the two inverter intervals (1 and 2), discussed above in detail, the transformer voltage remains positive. This period corresponds to the first rectifier interval (Table II) in which diode

Table II
Sequence and governing equations of the secondary rectifier intervals

U	Device	From	To	i _{DP}	i _{DN}	V _m	L*
1	D _p	i _{DN} ≤ 0	V _s ≤ $\frac{L_{1k}}{2} \frac{d}{dt} i_{DP}$	i _L	0	V _s	L + L _{1k}
2	D _p , D _n	V _s ≤ $\frac{L_{1k}}{2} \frac{d}{dt} i_{DP}$	i _{DP} ≤ 0	i _L - i _{DN}	$\frac{di}{dt} = \frac{-V_s}{L_{1k}}$	0	L
3	D _n	i _{DP} ≤ 0	V _s ≥ $-\frac{L_{1k}}{2} \frac{d}{dt} i_{DN}$	0	i _L	-V _s	L + L _{1k}
4	D _p , D _n	V _s ≥ $-\frac{L_{1k}}{2} \frac{d}{dt} i_{DN}$	i _{DN} ≤ 0	$\frac{di}{dt} = \frac{V_s}{L_{1k}}$	i _L - i _{DP}	0	L

D_p conducts. The next interval is reached only when the transformer voltage changes polarity and D_n gets forward biased. From Fig. 5a, the condition for D_n to be forward biased, can be derived as

$$-V_s \geq V_s - L_{lk} \frac{d}{dt} i_{Dp}. \quad (9)$$

During interval 2, known as the overlap interval, both D_p as well as D_n conduct, resulting in zero voltage across P and Q. The current through D_p decreases at the rate given by,

$$\frac{d}{dt} i_{Dp} = \frac{V_s}{L_{lk}} \quad (10)$$

and when it reaches zero, the next interval begins where D_n alone conducts. The equations valid in each of the four rectifier intervals are listed in Table II. The next section outlines the design strategy for achieving ZVS.

4. Design considerations to achieve ZVS

From the analysis of the PMC, it is important to note that there are two types of transitions. One is from the power transfer mode to the freewheeling mode (inverter intervals 2 and 6) and the other from the freewheeling to the power transfer mode (intervals 4 and 8). From the ZVS viewpoint, these two transitions are quite different. In the transition from power transfer to freewheeling mode, referred to as the right-leg transition, the reflected load current is always in the proper direction to discharge the capacitance of the MOSFET to be turned on. Hence the load current aids the magnetizing current in achieving ZVS. In the other transition, referred to as the left-leg transition, the reflected load current begins to reverse direction, the rate of reversal being determined by the leakage inductance. Once the load current reverses direction, it opposes the magnetizing current in the discharge of the MOSFET capacitance. Hence the left-leg transition is more critical from the ZVS standpoint. The design equations are, therefore, derived to achieve ZVS in this transition, which automatically ensures ZVS for the other transition too.

Apart from the magnetizing and leakage inductances, the other parameter which affects ZVS, is the dead time $[T_{Delay}]$ allowed between the turn-off of a MOSFET and the subsequent turn-on of the other MOSFET in the same arm. All the parameters along with their qualitative effects on ZVS are given in Table III.

From the equations valid for the fourth inverter interval (left-leg transition which is the crucial one for ZVS) the following expression can be derived⁴, for the voltage V_{C_2} across the MOSFET to be turned on

$$V_{C_2} = V_{DC} - (i_m + i_{ref}) \sqrt{\frac{L_{eq}}{2C}} \sin \omega t \quad (11)$$

Table III
Parameters affecting ZVS and their qualitative effects

Variable	Positive effect	Negative effect
Magnetizing current	Aids ZVS	Higher current stress and conduction loss
Leakage inductance	Aids ZVS, by reducing the rate of reversal of the primary current in the intervals 4 and 8	Reduces maximum effective duty ratio; hence poor VA utilisation and more conduction loss. Results in higher ringing and dissipation in secondary rectifiers.
T_{Delay}	Large T_{Delay} aids ZVS at light loads and affects adversely at high loads	Large T_{Delay} reduces the effective duty ratio and is particularly undesirable at very high switching frequencies.
Capacitance across the MOSFET- C_{DS}	Large C_{DS} aids in loss-less turn-off	Large C_{DS} demands more energy to be stored in the transformer inductances, to be fully discharged, hence bad for ZVS.

where

$$\omega = \frac{1}{\sqrt{2C \cdot L_{\text{eq}}}}$$

$$L_{\text{eq}} = L_{\text{Lk}}^* | L_{\text{m}}; (L_{\text{Lk}}^*, \text{leakage inductance referred to the primary}).$$

The above expression gives the following two conditions to achieve ZVS at any given load.

$$1. (i_m + i_{\text{refl}}) \sqrt{\frac{L_{\text{eq}}}{2C}} \geq V_{\text{DC}} \quad (12)$$

$$2. T_{\text{Delay}} = \frac{\pi}{2} \sqrt{2C L_{\text{eq}}} \quad (13)$$

The first condition ensures that the peak of the sinusoidal component of eqn (11) is at least equal to V_{DC} , so that V_{C_2} eventually reaches zero. The second condition ensures that the MOSFET is switched on when V_{C_2} is zero. Hence the design strategy is to

- select T_{Delay} considering the switching frequency and the MOSFET characteristics.
- calculate the value of L_{Lk} from eqn (13), with the above value of T_{Delay} .
- with the above value of L_{Lk} , calculate from eqn (12), the peak magnetizing current required at any load down to which ZVS is required.

The full system may be numerically simulated with the help of equations listed in Tables I and II, and using the above values for delay time, magnetizing current and leakage inductance as initial estimates. From repeated simulation runs, more satisfactory design values for all the parameters may be found.

5. Development of a 250 kHz/560 W offline converter

The design and development of a PMC of the following specifications are discussed.

Input : 150–270 V ac, 50 Hz

Output voltage	: 28 V
Maximum output current	: 20 A (nominal power = 560 W)
Output regulation	: 0.1%
Output ripple (peak to peak)	: 0.5%
Switching frequency	: 250 kHz

ZVS right down to no load, though possible, results in very high conduction losses. The reasons for the increased conduction losses are:

1. High magnetizing current.
2. Large leakage inductance resulting in reduced turns ratio.
3. Circulating peak primary currents during the freewheeling interval. This source of loss is particularly severe at very low duty ratios encountered in wide-input applications.

The first step in design is to decide the ZVS limit, *i.e.*, the load down to which ZVS is preferred. Figure 6 gives the MOSFET loss curves at various ZVS limits, corresponding to the given specifications and for the chosen MOSFET (IRFP 460) with $R_{DS\ ON}$ of $0.3\ \Omega$. The decision on ZVS limit may be made either to achieve the minimum possible heatsink size or to minimize the losses at any particular load or range of loads considered as nominal. In this design, the ZVS limit is chosen as 16 A (80%). The values of magnetizing and leakage inductances and T_{Delay} are then chosen according to the procedure outlined previously. They are listed in the section on experimental results. The designed values of magnetizing and leakage inductances are realised through separate external inductors initially. It is possible to integrate them into the power transformer by introducing appropriate air gap.

The transformer turns ratio is selected considering the maximum duty ratio available. High-frequency ferrite core materials are chosen for the transformer and the inductors.

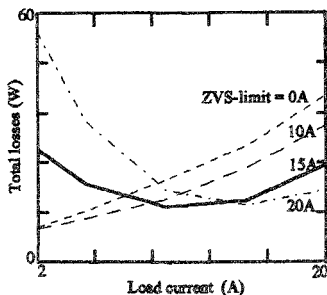


FIG. 6. Loss curves for various ZVS limits.

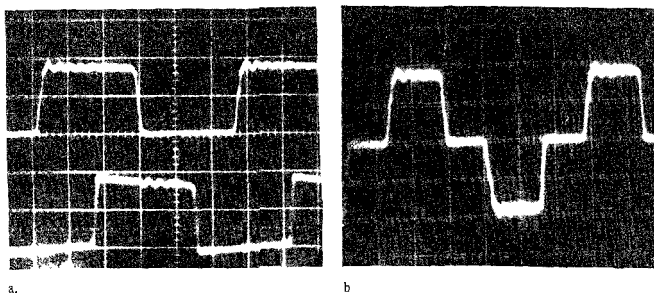


FIG. 7. Phase difference at 150 V ac input. a. V_A and V_B and b. V_{AB} (Vert: 125 V/div; Hori: 0.66 μ S/div).

They are operated at low-flux densities (< 0.1 T) to reduce the core losses. The windings are made with copper foils to reduce losses.

The phase-modulation controller IC, ML4818 is used to obtain the control signals. It features a programmable T_{Delay} . The driver stage consists of external P- and N-channel MOSFETs and is designed for fast turn-off (< 100 ns) to reduce the turn-off losses. The turn-on is made relatively slower, as it is a loss-less transition. The design of output LC filters and closed loop compensators is similar to that of PWM converters².

6. Experimental results

6.1. Output regulation by phase modulation

Output voltage regulation, better than 0.1% over the entire line and load ranges, is obtained by phase modulation. Figures 7 and 8 show how the phase difference is controlled to regulate the transformer primary voltage, as the input varies from 150 to 270 V ac.

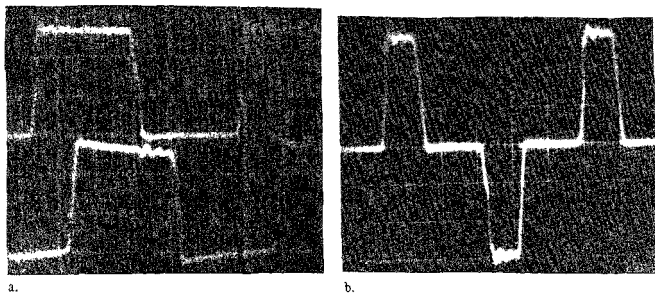


FIG. 8. Phase difference at 270 V ac input. a. V_A and V_B , and b. V_{AB} (Vert: 125 V/div; Hori: 0.66 μ S/div).

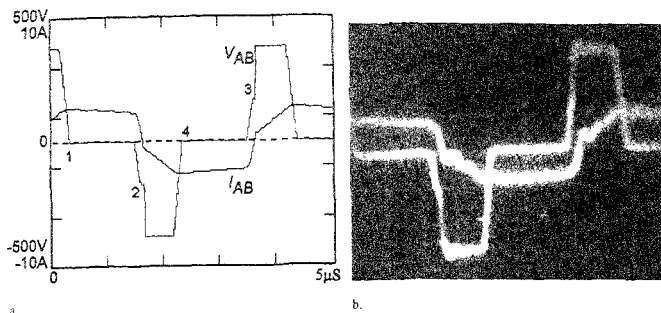


FIG. 9 Primary voltage and current at 6A load, showing the turn-on transients. a. simulated waveforms (1, 2, 3 and 4 represent the instants when S_1 , S_2 , S_3 and S_4 are switched on) and b. experimental results (V_{AB} : 125 V/div; I_{AB} : 2.5 A/div; Horz: 0.5 μ s/div).

6.2. ZVS and non-ZVS turn-on

The transformer primary voltage gives information about the turn-on transitions of all the four MOSFETs. Figure 9 shows the simulated and experimental waveforms of the transformer primary voltage (V_{AB}) and current (I_{AB}) corresponding to a load current of 6 A. As can be seen, the turn-on in the freewheeling to power transfer mode, takes place with about 180 V across the switch. This loss of ZVS is due to the insufficient energy stored in the transformer inductances. However, the turn-on in the other transition is ZVS. Figure 10 shows the same waveforms for a load current of 18 A. As seen, the increased reflected load current results in ZVS turn-on for all the transitions. Figure 11

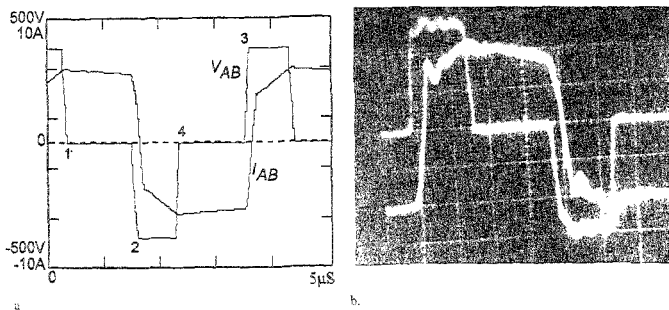


FIG. 10 Primary voltage and current at 18A load. All the transitions are ZVS a. Simulated waveforms and b. experimental results (V_{AB} : 125 V/div; I_{AB} : 2.5 A/div; Horz: 0.5 μ s/div)

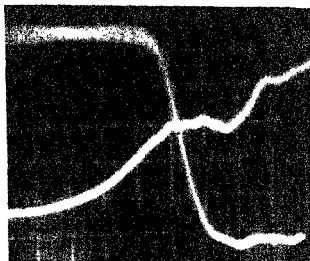


FIG. 11. V_{GS} and V_{DS} waveforms for ZVS transition. V_{GS} raises from -12 V towards $+12$ V. Note that V_{DS} drops to zero volts even before the gate voltage reaches the threshold (V_{DS} : 60 V/div; V_{GS} : 5 V/div; Hori: 50 ns/div).

shows the waveforms of the gate voltage and drain-source voltage, corresponding to ZVS turn-on. As can be seen, the drain-source voltage reaches zero, even before the gate voltage becomes positive. (Note that the gate voltage rises from -12 to $+12$ V).

6.3. ZVS limit and MOSFET losses

The ZVS limit chosen in the design is 16 A (80% load). The values obtained from simulation for the various parameters to obtain the chosen ZVS limit are listed below:

$$\begin{aligned} T_{\text{Delay}} &: 175 \text{ ns} \\ C_{\text{DS}} &: 600 \text{ pF (intrinsic} = 380 \text{ pF; external} = 220 \text{ pF)} \\ L_m &: 140 \text{ } \mu\text{H} \\ L_{\text{Lk}} &: 7 \text{ } \mu\text{H} \end{aligned}$$

With these values, ZVS is obtained from full load down to 16.6 A. By varying the magnetizing inductance, the performance of the converter under various ZVS limits is

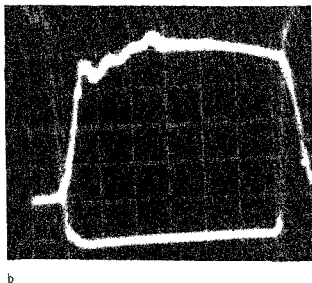
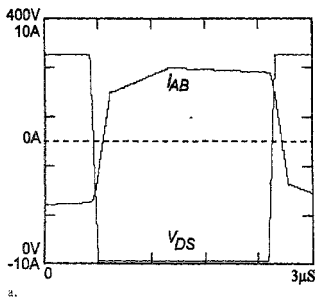


FIG. 12. V_{DS} vs I_{AB} for left-leg MOSFETs. I_{AB} is equal to the device current when V_{DS} is zero. Note that the device voltage falls to zero, before the current through it becomes positive a. simulated results and b. experimental results (V_{DS} : 60 V/div; I_{AB} : 2.5 A/div; Hori: 0.5 μs /div).

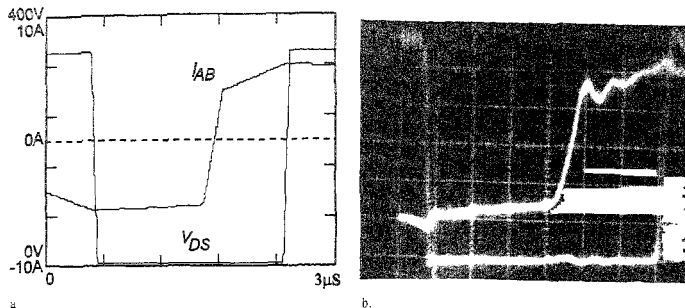


FIG. 13. V_{DS} vs I_{AB} for right-leg MOSFETs. The intrinsic diode conducts (negative current with V_{DS} zero) for the major part. a. simulated results, and b. experimental results (V_{DS} : 60 V/div; I_{AB} : 2.5 A/div; Hori: 0.5 μ s/div).

studied. The results thus obtained for two ZVS limits—60 and 80% load—are listed in Table IV and are compared with the simulation results.

6.4. Left- and right-leg transitions

As explained earlier, the left- and right-leg transitions are quite different from the ZVS viewpoint. In the left-leg MOSFETs, the intrinsic diode conducts only during the transients. In the right-leg MOSFETs, the diode conducts for almost as much time as the MOSFET channel. Achieving ZVS for these MOSFETs is relatively easier. Figures 12 and 13 show the MOSFET voltages and the primary current (which is equal to the device current when it is on) for the left- and right-leg MOSFETs, respectively.

6.5. Turn-off transition

The turn-off losses depend on the capacitances across the devices (intrinsic and external) and the fall time. Figure 14 shows the gate voltage and drain-source voltage waveforms

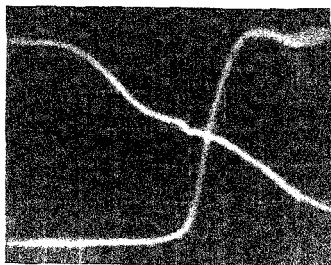


FIG. 14. V_{DS} vs V_{GS} during turn-off. V_{GS} falls from +12 V to -12 V (V_{DS} : 60 V/div; V_{GS} : 5 V/div; Hori: 50 ns/div).

Table IV
Converter performance for two different ZVS limits at the maximum input voltage

Parameters	ZVS limit = 12 A		ZVS limit = 16 A	
	Experimental	Simulation	Experimental	Simulation
Peak device voltage stress	400 V	380 V	400 V	380 V
Peak current stress	7.8 A	7 A	6.7 A	6 A
V_{DS} at turn-on				
Left-leg MOSFETs				
@ Min. load(2A)	215 V	188 V	280 V	276 V
Half load	80 V	74 V	153 V	146 V
Full load	0	0	0	0
Right-leg MOSFETs				
@ Min. load(2A)	120 V	100 V	195 V	190 V
Half load	0	0	0	0
Full load	0	0	0	0
Total power lost in all the MOSFETs				
@ Full load	27 W	29.5 W	22 W	23.1 W
Half load	14 W	13.2 W	15.5 W	14.2 W
Min. load (2A)	13 W	11.8 W	27 W	28.2 W
Full load efficiency	80.6%	—	82%	—

during the turn-off transition, at full load. The gate voltage falls from 12 to -12 V. By the time the gate voltage falls below the threshold of 2 V (representing zero device current), the V_{DS} rises only by about 30 V. Hence the turn-off losses are small.

6.6. Power density

Commercial power supplies with specifications similar to the one developed, but operating at 50 kHz, have power densities typically around 2 W/inch³. The developed phase-modulated converter operating at 250 kHz, has a power density close to 5 W/inch³. The major volume, as expected in high-frequency converters, is occupied by the heatsinks for the rectifier diodes and the primary MOSFETs. About 20% of the volume is used for the EMI filters, to meet the stringent specifications. The size of the magnetic components reduce by a factor of about 2.5 compared to 50 kHz converters. With the latest high-frequency core material, further reductions are possible.

Power densities above 30 W/inch³ have been reported in literature. However they cannot be readily compared with the commercial power supplies like the one developed, since the specifications in the two cases are quite different. Wide input ranges, stringent EMI specifications, many protection and monitoring requirements and the overrating of the components to increase reliability are some of the reasons for the low power densities in the commercial power supplies. However, if the components are chosen to optimise power density rather than cost, and with better engineering, power densities of 10 to 15 W/inch³ can be achieved with the phase-modulated topology.

7. Conclusions

With its ZVS characteristics and constant-frequency control, the phase-modulated full-bridge converter is well suited for high-voltage and high-power applications. Results obtained on a 560 W/250 kHz offline phase-modulated converter are presented to substantiate this claim.

The advantages of PMC are more striking in applications where the range of input variation is not too wide. One such important application area is in high-power converters with front-end power factor control (PFC) scheme.

ZVS limit, defined as the load down to which ZVS is obtained, is an important factor to be considered in the design. The optimum choice depends on many parameters like operating frequency, MOSFET characteristics like $R_{DS\ ON}$, input voltage variations, etc., apart from cost and size considerations. Digital simulation is a very useful tool in deciding and then designing for the most satisfactory value of ZVS limit, for any particular application.

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References

1. MILLER, E. J. Resonant switching power conversion, *IEEE Proc Power Electronics Specialists Conf 1976 Record*, pp. 206–211.
2. LIU, K., ORUGANTI, R. AND LEE, F. C. Resonant switches: Topologies and characteristics, *IEEE Proc Power Electronics Specialists Conf. 1985 Record*, pp. 106–116.
3. HUA, G., LEU, C. AND LEE, F. C. Novel zero voltage transition PWM converter, *IEEE Proc. Power Electronics Specialists Conf. 1992 Record*, pp. 55–61.
4. RAJAPANDIAN, A. *A constant frequency resonant transition converter*, M. Sc. Thesis, Deptt of Electrical Engineering, Indian Institute of Science, Bangalore, India, 1995.
5. MOHAN, N., UNDELAND, T. M. AND ROBBINS, W. P. *Power electronics: Converters, applications and design*, pp. 229–245, 1989, Wiley.