

Designing for zero-voltage switching in phase-modulated series resonant converters

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Abstract

Achieving soft switching in switched-mode power supplies is an important design criterion today. Converters like the series-loaded resonant topologies are preferred because they easily enable soft switching. However, the soft switching range is limited and depends on a number of parameters that are not directly under the designer's control. Special design rules are used to arrive at the optimum operating points and thus maintain soft switching over at least a major portion of the operating range. This paper deals with the design issues relevant to achieve zero-voltage switching (ZVS) for the phase-modulated series resonant converter. The ZVS mechanism and the modes of operation for which the converter inherently offers ZVS are explained. A circuit modification to extend the ZVS range beyond the natural range of the converter is introduced. Further, the design procedure for achieving ZVS is discussed through a design example. A phase-modulated series resonant converter for high-voltage DC applications is designed and experimentally shown to have ZVS over its entire specified operating range.

Keywords: Soft switching, zero-voltage switching, resonant converters, high-voltage power supplies, phase modulation.

1. Introduction

The series resonant converter (SRC) is a load resonant converter that finds usage in high-power conversion applications like ship propulsion, electric traction and in special applications like high-voltage output DC–DC converters. Large transformer parasites are typical of these converters. For example, the leakage inductance of the high-voltage transformer in a high-voltage DC–DC converter is large enough to prevent sufficient power flow from the source to the load. Introducing a capacitor in series with the parasitic leakage inductance results in a series LC circuit. The effective impedance offered to the power flow is then reduced if the converter is operated with a switching frequency close to that of the resonant frequency of the series LC circuit. The classical SRC is a frequency-controlled converter. That is, control is achieved by varying the switching frequency with respect to the converter's resonant frequency. Control can also be achieved by varying the duty cycle. Such an SRC, having a fixed switching frequency but variable duty ratio, is called the phase-modulated series resonant converter (PM-SRC) (Fig. 1). The term PM-SRC is adopted because the PWM inverter output voltage is obtained using the phase modulation technique.

One of the critical design issues in any switched-mode power supply is achieving soft switching over the entire operating range of the converter. A soft-switched converter has lower

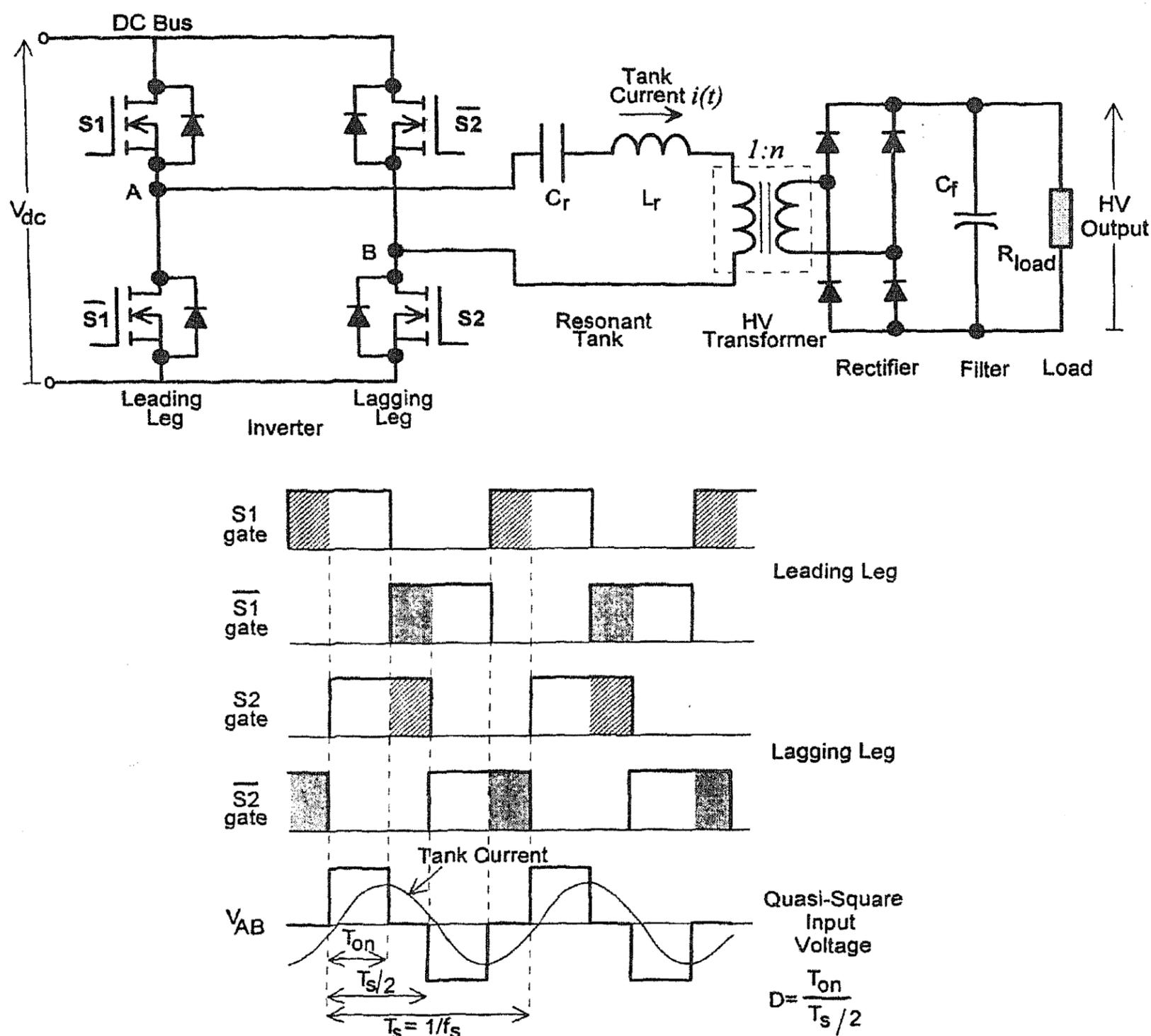


FIG. 1. Schematic of the phase-modulated series resonant converter for high-voltage applications.

generated EMI, switching losses and stress on the power switches. The lower switching losses promote higher switching frequency, which further results in overall size and cost reductions. Though one of the positive features of the SRC is that it enables soft switching, the soft-switched operating regions are limited and depend on a large number of parameters, including the load. Proper design is therefore required to ensure soft switching over the defined operating range.

This paper explains the design issues critical for achieving soft switching in MOSFET-based PM-SRC operating above the resonant frequency. The paper discusses how zero-voltage switching (ZVS) is achieved and its operating zones. A modified circuit to extend the range of ZVS is described. Design relations for achieving ZVS are explained through a design example.

A PM-SRC used for high-voltage DC generation is designed for ZVS over its entire load range and experimental results are provided to validate the design.

2. PM-SRC Circuit description and operation

The PM-SRC (Fig. 1) is also referred to as the phase-shift-controlled or pulse-width-modulated SRC in the literature.^{1, 2} The PM-SRC consists of a full bridge inverter feeding a quasisquare voltage waveform to a series resonant tank. The resonant tank consists of the resonant inductor (L_r) and the resonant capacitor (C_r). The resonant inductor value is the sum of the transformer leakage inductance and any external inductor if present. The resulting resonant tank will have a resonant frequency (f_r) given by

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \quad (1)$$

Another parameter that characterises the resonant tank is its characteristic impedance, Z_c . By definition,

$$Z_c = \sqrt{\frac{L_r}{C_r}}. \quad (2)$$

Switching frequency (f_s) of the inverter is kept constant while the duty ratio (D) is varied using phase modulation technique. Therefore, the resonant tank is excited by a quasisquare waveform having frequency f_s and duty ratio D . The excitation results in a sinusoidal or near-sinusoidal current in the resonant tank. The tank current ($i(t)$) is rectified by a diode bridge rectifier and filtered using capacitive filter to get the required output voltage. The magnitude of the output voltage depends on the magnitude and wave shape of $i(t)$ and the load (R_{load} in Fig. 1). The magnitude and wave shape of the resonant tank current depends on f_s , D and the load factor (Q) of the converter. By definition, Q is the ratio of the resonant tank characteristic impedance and the resistive load as seen from the resonant tank. That is,

$$Q = \frac{Z_c}{R_{pri}}, \quad (3)$$

where $R_{pri} = R_{load}/n^2$ is load as seen by the resonant tank and n is high-voltage transformer turns ratio.

The operating frequency (f_s) is generally close to the resonant frequency of the tank. Operation with $f_s < f_r$ is called the below resonant frequency operation. The input voltage then sees a net capacitive tank circuit.³ When $f_s > f_r$, the operation is termed above resonant frequency and the tank presents a net inductive circuit.³ The above resonant frequency operation facilitates ZVS for the inverter devices while the below resonant frequency operation promotes ZCS (zero-current switching).

For phase modulation,⁴ a full bridge inverter with fully controlled devices is required (Fig. 1). Each device is switched at 50% duty ratio with the high- and low-side devices of the same leg being complementary. As shown in waveforms of Fig. 1, conduction of switches on the leading leg of the inverter (S_1, \bar{S}_1) is phase-shifted with respect to the conduction of switches

on the lagging leg (S_2, \bar{S}_2), resulting in the quasisquare input voltage. Here, the inverter leg containing the devices that turn on first (S_1, \bar{S}_1) is termed as the 'leading leg' and the other leg is termed as the 'lagging leg.'

3. Zero-voltage switching in PM-SRC

As mentioned earlier, when the PM-SRC is operated such that its switching frequency is greater than the resonant frequency of the tank, zero-voltage turn-on of the inverter devices is possible. The latter is preferred over zero-current turn-off in MOSFET-based converters. ZVS ensures that the inherent output capacitance in the MOSFET switch is discharged prior to switch turn-on, thus preventing turn-on losses and generated EMI. Figure 2 shows how ZVS is achieved for the switch \bar{S}_1 . The high-side MOSFET S_1 is turned off at time T_{1_a} (Fig. 2(b)) when the tank current $i(t)$ still flows through it. Because of the resonant inductance, $i(t)$ is not interrupted. The tank current is maintained through the snubber capacitors across the switches on the leading leg (S_1 and \bar{S}_1), thus charging C_{11} to V_{dc} and discharging C_{12} . The inherent body diode of the MOSFET \bar{S}_1 turns on (Fig. 2(c)) once the voltage across C_{12} reaches the diode forward break over voltage. The tank current presently freewheels through the body diode of \bar{S}_1 , the resonant tank and the still conducting lagging-leg switch S_2 . The voltage across S_1 is the diode drop and is nearly zero. Applying the gate pulse to turn on \bar{S}_1 during this period (at time T_{1_b}) results in zero-voltage turn-on. The switch \bar{S}_1 being a MOSFET will conduct $i(t)$ in the reverse direction as soon as its gate pulse is applied (as indicated in Fig. 2(d)).

The turn-on process is therefore lossless and stress-free. Turn-off occurs when a sizeable current flows through the switches. But the rate of voltage rise across the switch is limited by the snubber capacitors across it. The snubber capacitors are subsequently discharged through the load (thus preventing snubber losses) prior to the switch turn-on. Therefore, the turn-off process also has low losses.

Zero-voltage turn-on sequence of the other three switches of the converter is similar. The basic requirements for achieving ZVS and low loss turn-off are therefore:

- The device should turn off with a positive current flowing through it.
- The turn-off current should be large enough to completely charge/discharge the snubber capacitors across the devices and subsequently turn on the diode across the device coming into conduction.
- There should be a time delay (T_D) between the turn-off of a device and the turn-on of the complementary device on the same leg. In the example above, $T_D = (T_{1_b} - T_{1_a})$.
- T_D should be large enough to allow the complete charging/discharging of the snubber capacitors and turning on of the antiparallel diodes but small enough to ensure that the tank current does not change direction before the device is turned on.
- Snubber capacitors should be large enough to prevent high dv/dt for the largest turn-off current, but small enough to be charged/discharged by the smallest turn-off current in the given time delay.

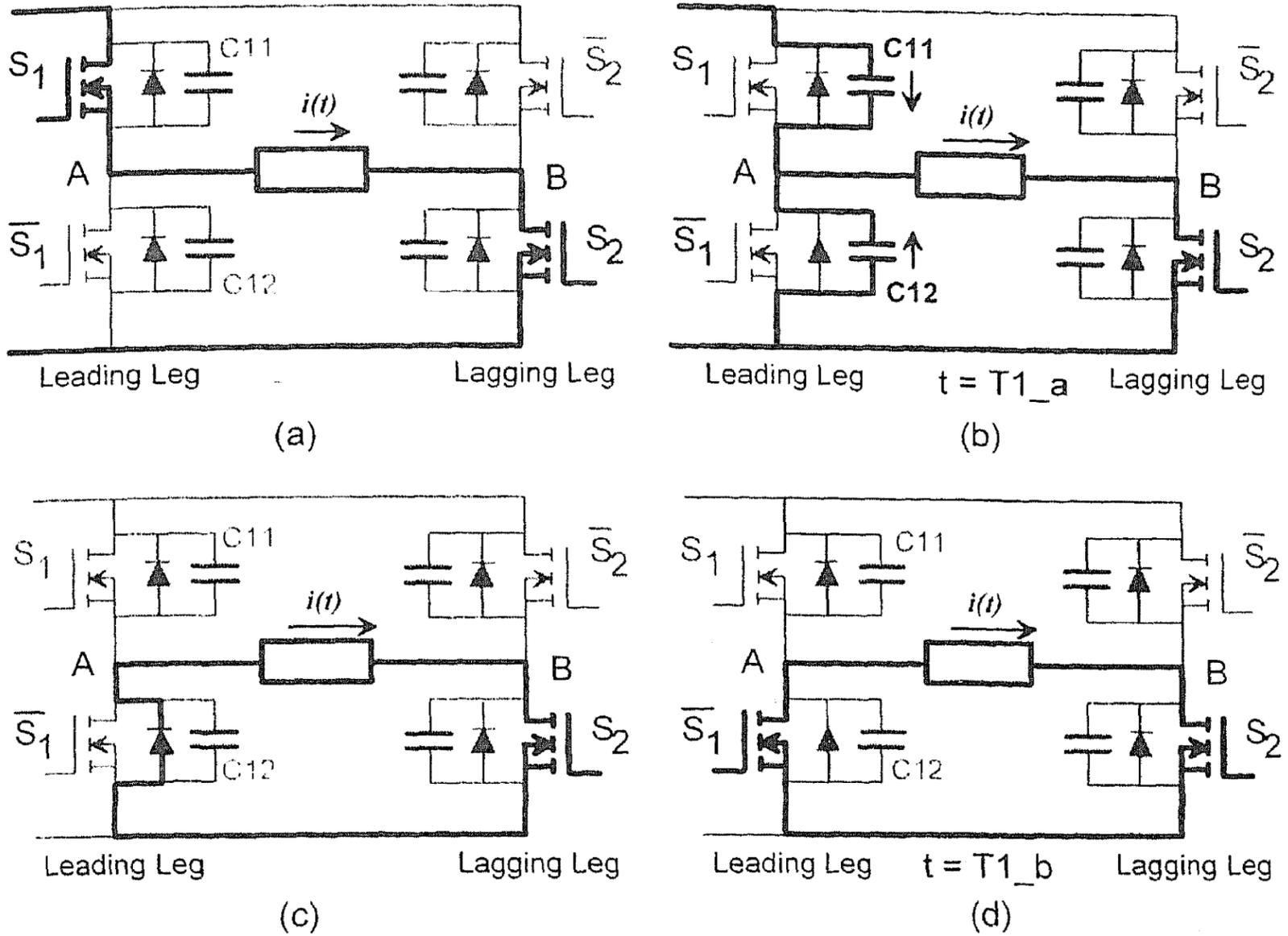


FIG. 2. Zero-voltage turn-on sequence for MOSFET \bar{S}_1 . The current paths are shown in dark.

4. Operating modes of the PM-SRC

Under steady state, the PM-SRC operating above the resonant frequency has three modes of operation as indicated in Fig. 3. Mode 1 is a continuous conduction mode. Its operation results for high Q , high D or when the f_s/f_r ratio is high. All the four devices turn off when a positive current flows through them. ZVS is therefore easily achievable over almost the entire range of Mode 1. The exceptions are at lower loads when the lagging-leg switches do not turn off enough current to completely charge/discharge the snubber capacitors.

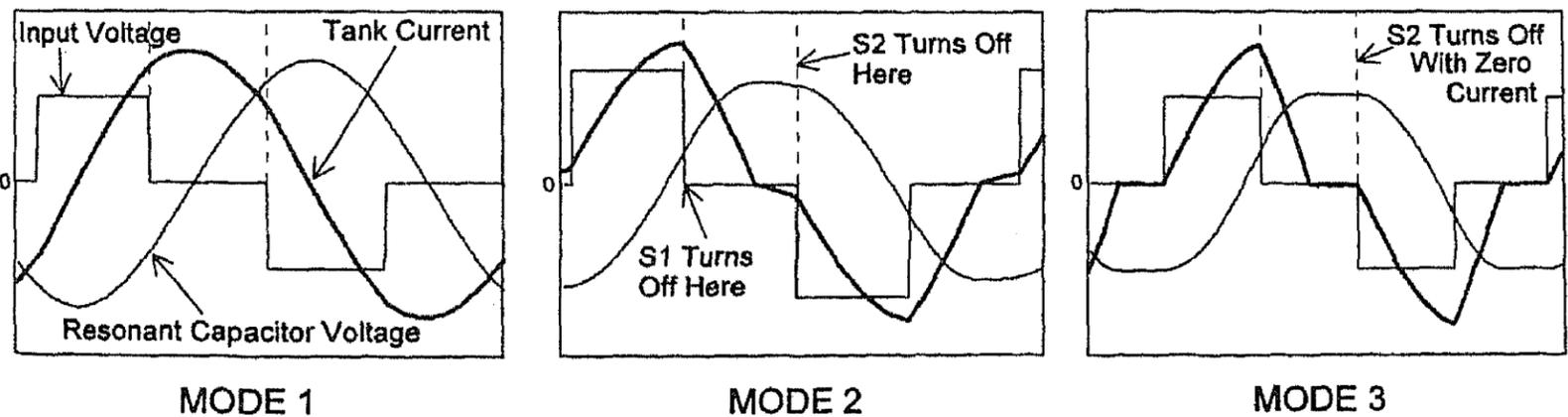


FIG. 3. The three modes of operation of the PM-SRC operating above the resonant frequency.

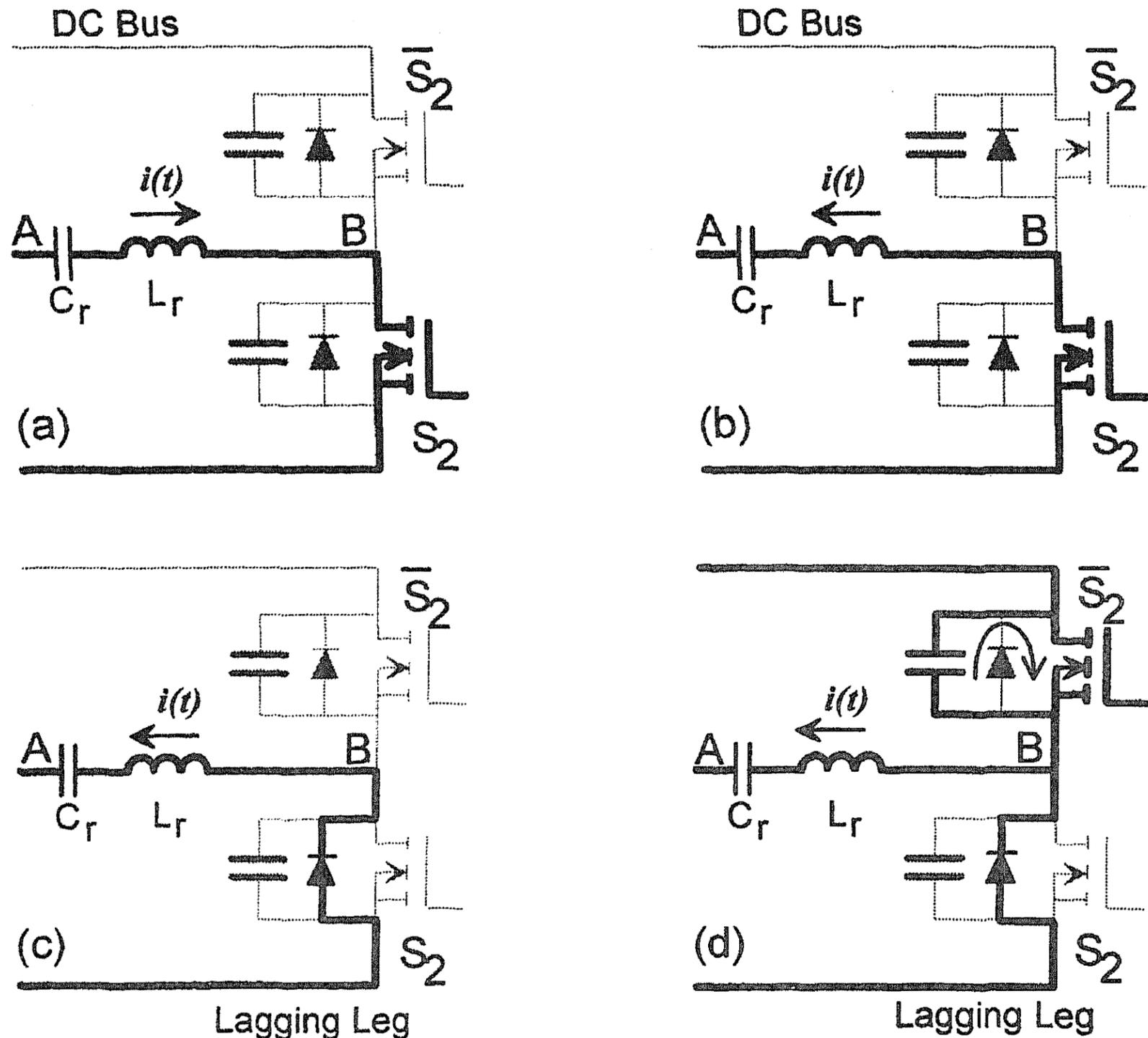


FIG. 4. Sequence showing loss of ZVS and turn-on stress on the lagging leg for a Mode 2 operation. The current paths are shown in dark.

The leading-leg switches turn off with a positive current for Mode 2 operation. However, the lagging-leg switches turn off with a negative current, i.e. after the tank current has reversed direction. Figure 4 gives the sequence of lagging-leg turn-off for Mode 2 operation. The tank current $i(t)$ reverses direction before the lagging-leg switch (S_2) is turned off (Fig. 4(b)). Since the gate pulse is still present for S_2 , it conducts in the reverse direction. Once the gate pulse to S_2 is removed, its inherent body diode takes over the tank current (Fig. 4(c)). The switch \bar{S}_2 is turned on after a time delay from the turn-off of S_2 (Fig. 4(d)). The S_2 body diode is force-commutated and the snubber across the device turning on (\bar{S}_2) dumps its charge through the device. The result is turn-on losses and generated EMI. Further, for high DC bus voltages there can be a false turn-on of S_2 due to Miller capacitance, leading to a shoot through. Figure 5 shows the oscilloscope plot of a lagging-leg switch commutation during Mode 2 operation. Clearly, Mode 2 operation is to be avoided.

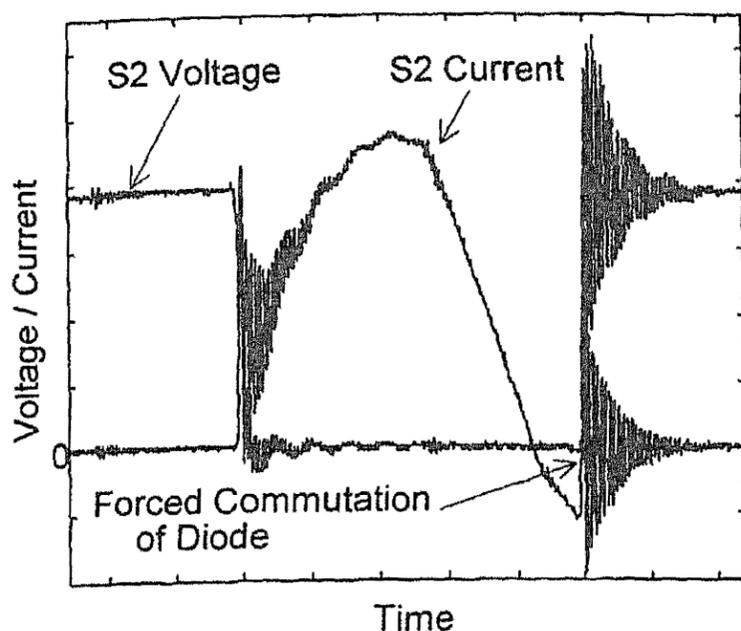


FIG. 5. Oscilloscope plot of the lagging switch transients for a Mode 2 operation.

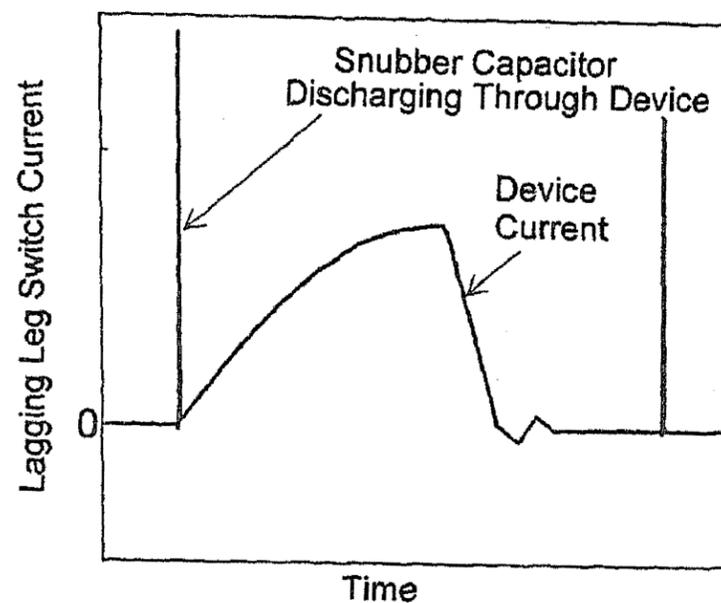


FIG. 6. Simulated waveform of lagging leg device current during Mode 3. ZCS ensures low loss and low stress turn off, but snubbers discharge through the device during turn on.

Mode 3 is a discontinuous operating mode resulting when $Q < (2/\pi)(f_s/f_r)$.⁵ The leading-leg switches turn off with a positive current; however, the turn-off current may be too low to charge/discharge even the MOSFET output capacitance. The lagging-leg devices turn off at zero current. Lagging-leg turn-off stress and losses are low because of ZCS; however, the lagging-leg snubber capacitors dump their charge through the device, leading to generated EMI and turn-on losses (Fig. 6). Though not as severe as the Mode 2 turn-off transients, Mode 3 operation too has to be avoided because of the generated EMI.

Figure 7 gives the operating mode boundaries⁵ for different loads (Q) and duty ratios (D) when $f_s/f_r = 1.1$. The thick line traversing through the plot indicates the operating point for maintaining a constant nominal output voltage when the load is changing. For the plot considered in Fig. 7, the nominal output voltage is $0.6 V_{dc}$ and the maximum load corresponds to

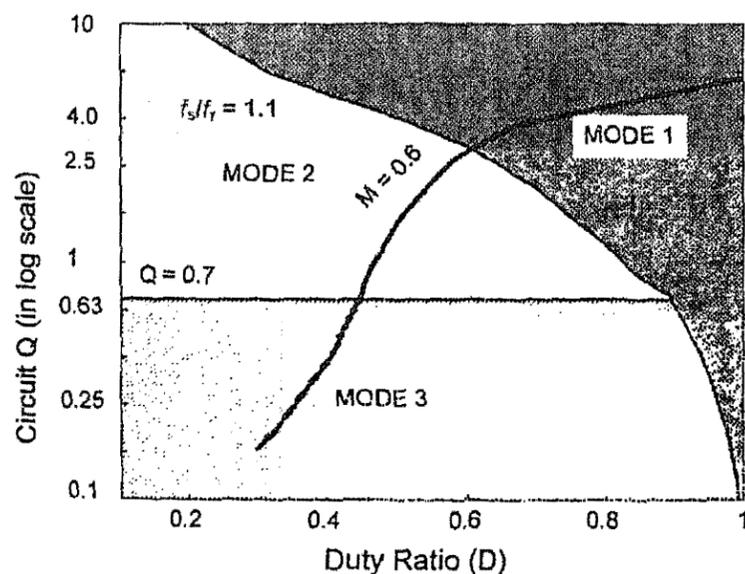


FIG. 7. Mode boundaries for $f_s/f_r = 1.1$. Obtained using mathematical analysis.

$Q = 6$. Mode 1 operation is lost below about 60% of the nominal load. If the load is between 17.5% and 60% of the nominal, the operation falls in Mode 2, while lower load results in Mode 3 operation. Figure 8 gives similar mode boundary plots for different f_s/f_r ratios. As seen, Mode 2 region decreases as the switching frequency moves away from the resonant frequency (higher f_s/f_r).

Mode 2 operation can be avoided by selecting high values for the nominal Q or by operating the converter farther away from the resonant frequency. The former results in large peak currents and voltages and lower voltage gain. The latter solution decreases the converter response time, the power delivered and the voltage gain, and has lower efficiency because of the relatively higher switching frequency.

Achieving ZVS for the lagging-leg devices is a more critical issue than the leading-leg devices. As seen above, the leading-leg devices turn off with a positive current under all operating conditions. ZVS can then almost always be designed except when the turn-off current is too low. On the other hand, the lagging-leg devices turn off with negative or zero current in Mode 2 and Mode 3, respectively. Thus, circuit modifications are necessitated to ensure ZVS in these operating modes.

5. Extending ZVS range using external inductor

A method of increasing the ZVS range of phase-modulated resonant transition converter by including an external inductive circuit⁶ was introduced earlier. This method can be extended to the PM-SRC and the disadvantages of Mode 2 and Mode 3 operations as discussed in the previous section can be eliminated⁵ (Fig. 9). An external inductor L_{ex} is connected between point B of the lagging leg and point E, which is a node with stiff voltage $V_{dc}/2$ maintained by the large divider capacitors C_{ex1} and C_{ex2} . Since S_2 and \bar{S}_2 are complementary to each other, the voltage V_{EB} across L_{ex} is a square-wave switching between $\pm V_{dc}/2$ at the switching frequency of the converter (f_s). The sum of the external inductor current $i_{ex}(t)$ and the tank current $i(t)$ flows through the lagging-leg switches. The peak negative turn-off current and the peak external inductor current ($I_{ex(peak)}$) coincide and by proper design, the net current flowing through the switches can be made non-negative.

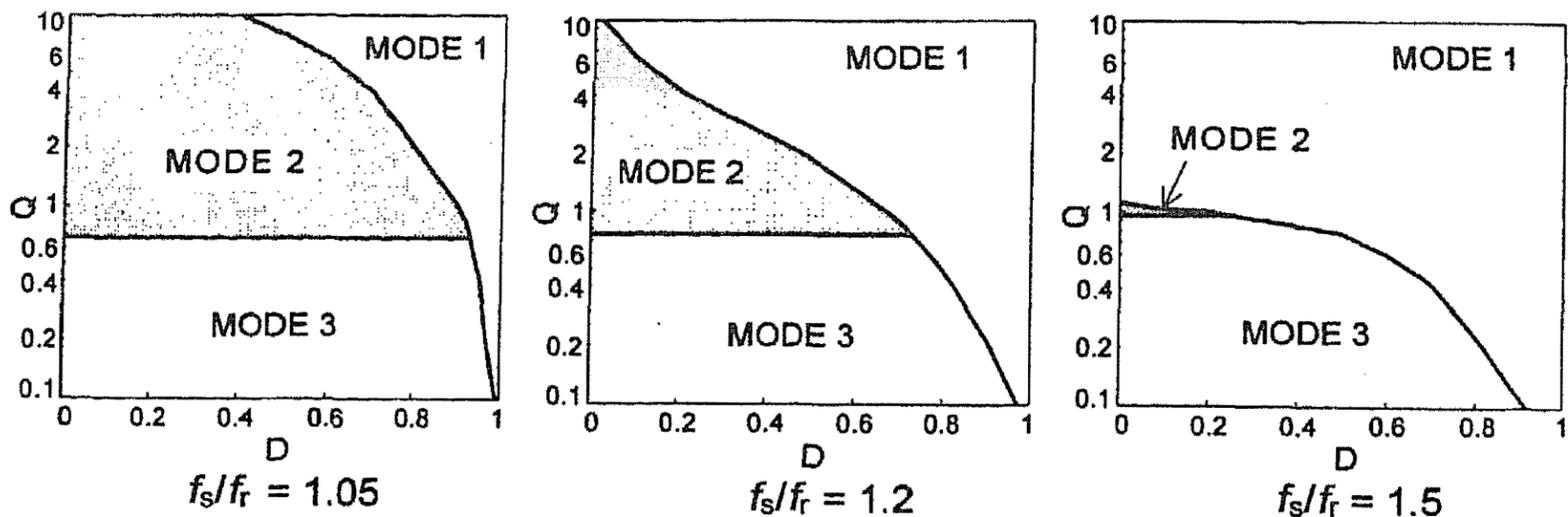


FIG. 8. Variation of the mode boundaries with changing f_s/f_r . Mode 2 region is reduced as f_s/f_r increases. Obtained through mathematical analysis.

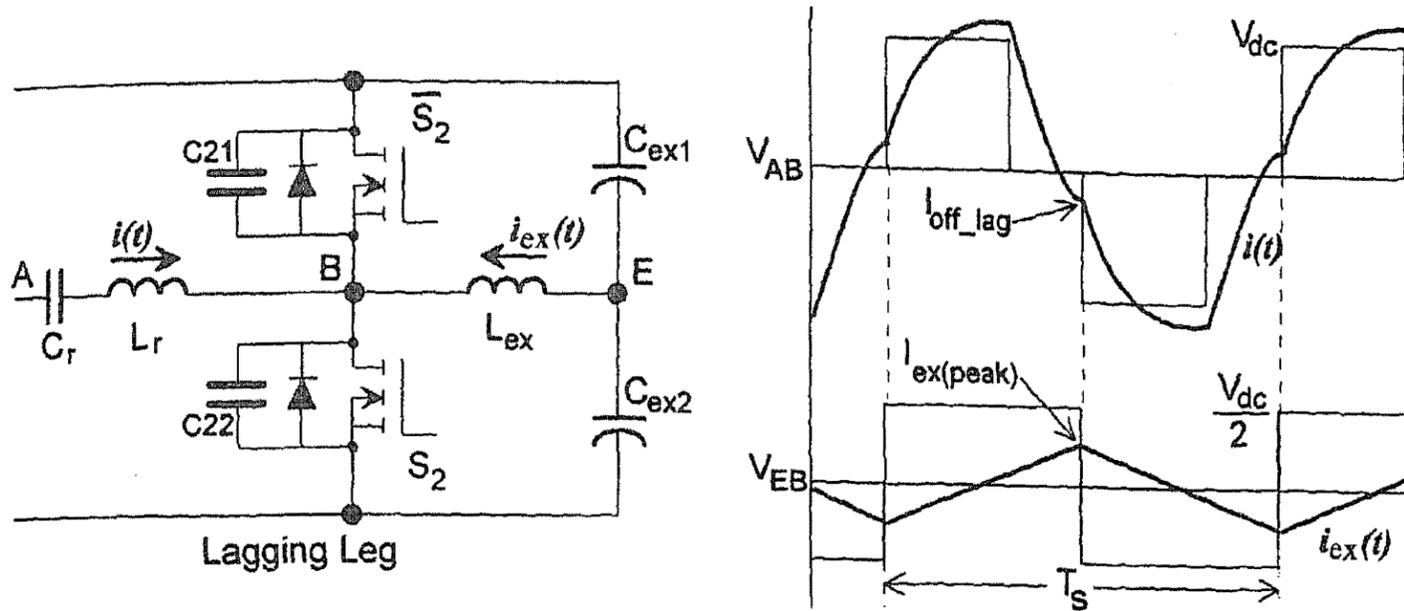


FIG. 9. Schematic of the modified circuit to aid in ZVS.

The ideal design to restore ZVS is: $I_{ex(peak)} = \text{maximum negative turn-off current plus the minimum current needed to discharge the snubber capacitors across the switch coming into conduction and charge the one across the switch turning off}$. For a given turn-off delay time T_{D_lag} and snubber capacitance C_{lag} , the current required (assumed constant during the delay time) for complete charge/discharge of the snubber capacitance is

$$I'_{off_lag} = \frac{2C_{lag} V_{dc}}{T_{D_lag}} \quad (4)$$

Then for an original turn-off current of I_{off_lag} (which is negative for Mode 2 and zero for Mode 3), the peak external inductor current to restore ZVS is

$$I_{ex(peak)} = |I_{off_lag}| + I'_{off_lag} = |I_{off_lag}| + \frac{2C_{lag} V_{dc}}{T_{D_lag}} \quad (5)$$

Using (5) and the basic inductor equation, the value of the external inductor is

$$L_{ex} = \frac{V_{dc}}{8f_s I_{ex(peak)}} \quad (6)$$

The original turn-off current I_{off_lag} is determined from the mathematical analysis or numerical simulation of the PM-SRC. Capacitor C_{lag} is chosen depending on the maximum turn-off current possible for the Mode 1 operation. The actual design is treated in the following sections.

SPICE simulation waveforms for a typical circuit with the external inductor ZVS aid are given in Fig. 10. The switch current is now the sum of the tank and external inductor currents. Figure 11 shows noticeable improvement in the oscilloscope plot of switch turn-off transients for Mode 2 operation when the external inductive circuit is included.

Inclusion of the external inductor does not influence the tank current and thus the analysis for the modified PM-SRC remains the same. Since there are ideally no lossy components in the

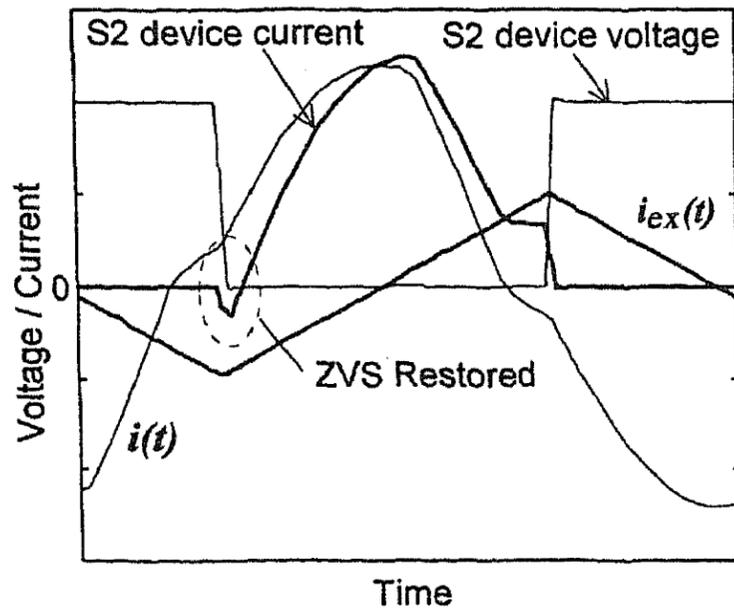


FIG. 10. SPICE simulation waveforms for the modified PM-SRC.

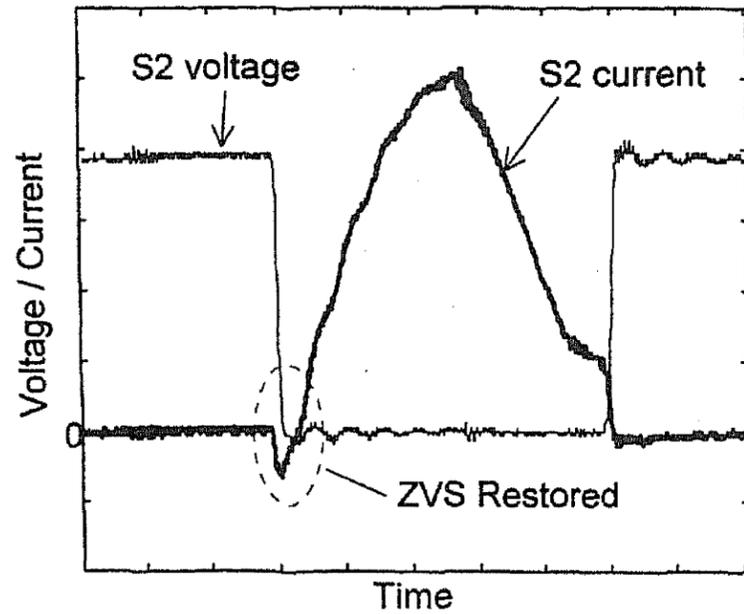


FIG. 11. Oscilloscope plot of the improved lagging leg switch transients on including the new modification.

path of $i_{ex}(t)$, there is no power loss associated with the modification. Peak current through the switches S_2 and \bar{S}_2 increases, leading to slight increase in conduction loss. But this is more than offset by the improved commutation.

6. Designing for ZVS

The actual design for ZVS is explained here through an example design for a PM-SRC for high-voltage DC output. Converter specifications are as given in Table I. The converter nominal operating points, currents and switch turn-off currents are arrived at through mathematical analysis. Device output capacitance indicated in Table I corresponds to the selected MOSFET switch.

6.1. Leading-leg snubber capacitor and time delay

The leading-leg snubber capacitor ($C_{lead} = C_{11}$ or $C_{12} + \text{MOSFET output capacitance}$) is chosen large enough to slow down the voltage rise for the largest turn-off current, thereby reducing turn-off losses. At the same time it should be small enough to be completely charged/

Table I
Specifications of the experimental converter

Variable	Nominal value
Input voltage	40 V DC
Output voltage	1000 V DC
Switching frequency (f_s)	100 kHz
Nominal output power	200 W
Minimum output power	20 W (10%)
Nominal voltage gain (primary side)	0.625
Frequency ratio f_s/f_r	1.1
Nominal load factor (Q)	4
Inverter device output capacitance	1.1 nF

discharged within the prefixed delay time by the smallest turn-off current. The maximum turn-off current occurs at the maximum load condition:

$$I_{\text{off_lead(max)}} = 13.6 \text{ A.}$$

For the short duration corresponding to the turn-off transient, it is assumed that the turn-off current will remain constant. Data sheets of the selected MOSFET give the typical device current fall time, t_f . Using the basic capacitor equation, the snubber capacitor value is obtained as

$$C_{\text{lead}} = \frac{I_{\text{off_lead(max)}} t_f}{2V_{\text{dc}}} = \frac{13.6 \times 50 \text{ ns}}{2 \times 40} = 8.5 \text{ nF.} \quad (7)$$

$C_{11} = C_{12} = 7.4 \text{ nF}$ (the rest provided by the MOSFET output capacitance).

The minimum turn-off current corresponds to the minimum load (chosen here as 10% of the maximum load, $Q = 0.4$, Mode 3 operation). Below this, ZVS is lost for the leading-leg switches.

$$I_{\text{off_lead(min)}} = 2.25 \text{ A.}$$

The time required to discharge C_{lead} is the delay time for the leading leg. Again, using the basic capacitor equation, this is determined as

$$T_{\text{D_lead}} = \frac{2C_{\text{lead}} V_{\text{dc}}}{I_{\text{off_lead(min)}}} \cong 300 \text{ ns.} \quad (8)$$

$I_{\text{off_lead}}$ is assumed to remain constant over the delay time $T_{\text{D_lead}}$ and the actual charge available to charge/discharge C_{lead} is the shaded area in Fig. 12. An amount of charge equalling the hatched area is now not available. Time T_2 is the crossover time for Mode 3 and is available from the mathematical analysis data or from numerical simulation. Approximating the area KLM to be a right triangle,

$$\text{available charge} = (I_r)(T_{\text{D_lead}}) + 0.5(I_{\text{off_lead(min)}} - I_r)(T_{\text{D_lead}}) = 600 \text{ nC.} \quad (9)$$

On the other hand, the charge required $= 2C_{\text{lead}} V_{\text{dc}} = 680 \text{ nC}$. The selected delay time is therefore increased slightly to $T_{\text{D_lead}} = 350 \text{ ns}$.

6.2. Lagging-leg snubber capacitor and time delay

For the lagging leg, the maximum turn-off current for the unmodified converter is

$$I_{\text{off_lag(max)}} = 3.4 \text{ A.}$$

However, this value will be later revised to a higher value because of the additional current from the external inductor circuit. The external inductive circuit adds an extra current so as to make the negative turn-off currents of Mode 2 positive. Once again from the analysis data, the maximum negative turn-off current occurs for $Q = 3$ and $D = 0.3$ (this does not correspond to the nominal gain of 0.625, but is chosen so as to eliminate the detrimental negative turn-off current for any operating condition).

$$|I_{\text{off_lag(neg)}}| = 1.73 \text{ A.}$$

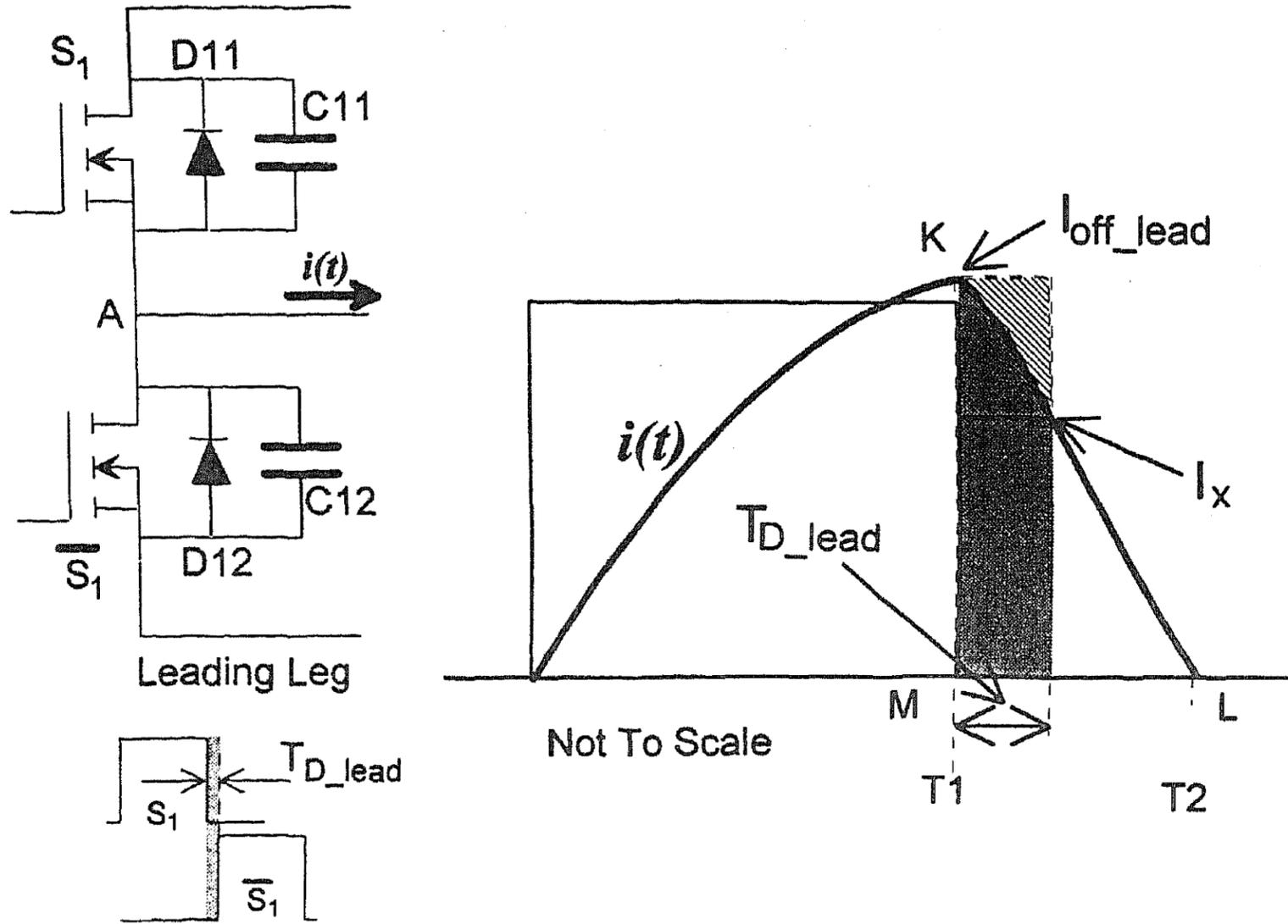


FIG. 12. Leading leg switch turns off at T_1 with a current $I_{\text{off_lead}}$. For the design, it is assumed that the turn-off current remains constant for the duration T_{D_lead} . However, an amount of charge equalling the hatched area is actually not available.

Referring to eqn (5) and the capacitor equation

$$C_{\text{lag}} = \frac{(I_{\text{ex (peak)}} + I_{\text{off_lag (max)}})t_f}{2V_{\text{dc}}}$$

$$\Rightarrow C_{\text{lag}} = \frac{(|I_{\text{off_lag (neg)}}| + I_{\text{off_lag (max)}})t_f}{2V_{\text{dc}}} \left(\frac{T_{D_lag}}{T_{D_lag} - t_f} \right) = 3.7 \text{ nF.} \quad (10)$$

$$C_{21} = C_{22} = 2.6 \text{ nF.}$$

Therefore, the minimum current required to charge/discharge C_{lag} is

$$I_{\text{off_lag (min)}} = \frac{2C_{\text{lag}}V_{\text{dc}}}{T_{D_lag}} = \frac{2 \times 3.7 \text{ nF} \times 40}{350 \text{ ns}} = 0.85 \text{ A.} \quad (11)$$

Since the minimum turn-off current can be selected by suitably designing the external inductive circuit, one has the freedom to choose the delay time for the lagging-leg switches. In (10)

Table II
Comparison of the calculated and the fine-tuned values

	C_{lead}^* (nF)	C_{lag}^* (nF)	L_{ex} (μH)	$T_{\text{D_lead}}$ & $T_{\text{D_lag}}$ (ns)
Initial calculation	8.5	3.7	19	350
Alteration after SPICE simulation	7.8	2.2	13	380
Final fine-tuned value	6.1	2.1	12.2	360

*includes MOSFET output capacitance of 1.1 nF

and (11) above, $T_{\text{D_lag}} = T_{\text{D_lead}} = 350$ ns. In case the control circuit has provision for setting different values for the delay times, $T_{\text{D_lag}}$ can be chosen as a smaller value.

The external inductor (Fig. 9) value is calculated from (5), (6) and (10) as

$$L_{\text{ex}} = \frac{V_{\text{dc}}}{8f_s I_{\text{ex (peak)}}} = \frac{40}{8 \times 100 \text{ kHz} \times (1.73 + 0.85)} = 19 \mu\text{H}. \quad (12)$$

L_{ex} is decreased by a small amount to increase the minimum turn-off current so that the error due to the constant current turn-off assumption is eliminated.

6.3. Fine-tuning the designed values

The design done above assumes ideal conditions and the values for the snubber capacitors, delay times and the external inductor have to be fine-tuned. The factors contributing to the non-idealities are:

- The circuit parasitics which change the switch currents and operating points.
- Parasitic transformer capacitance of the high-voltage transformer, which has a significant influence on the switch turn-off currents.
- Lower voltage across the external inductor circuit owing to conduction drop across the devices.
- Limited values for the snubber capacitors and their tolerance levels.

The converter with ZVS aiding components designed above is simulated using circuit-based simulation tools. Besides using models of the selected components, the measured circuit non-idealities are included. Based on this, the actual values used in the prototype are listed in Table II.

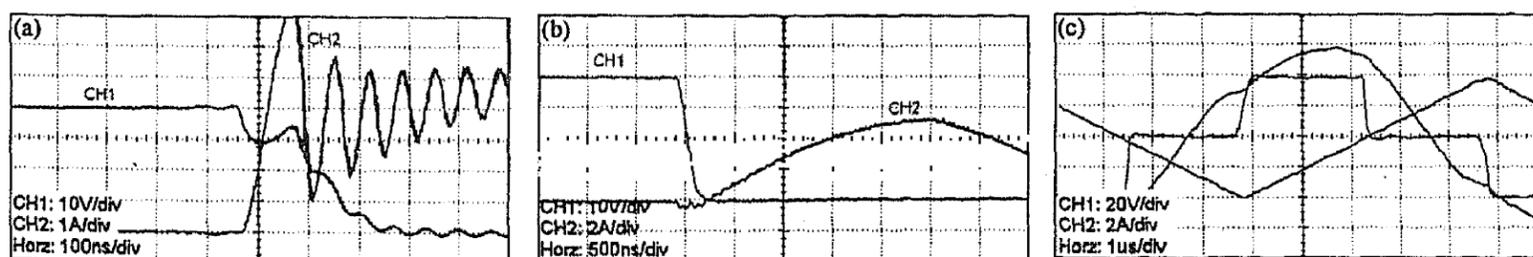


FIG. 13. Oscilloscope plots. (a) Lagging leg turn-on without the external inductor circuit, (b) with the external inductor circuit and (c) External inductor circuit current, resonant tank current and input voltage waveform.

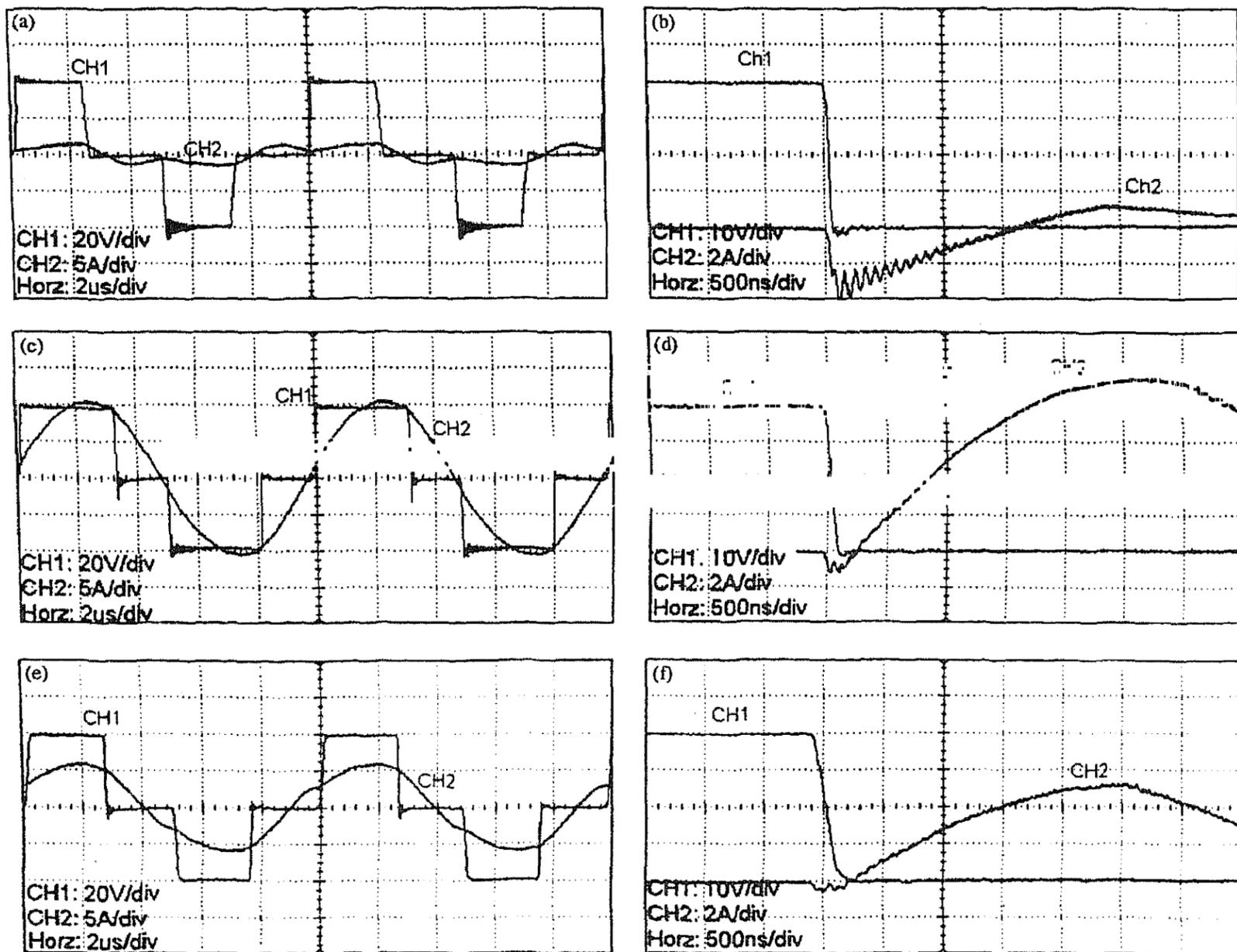


FIG. 14. Oscilloscope plots. Tank current waveform for (a) 100% (c) 50% and (e) 10% loads; Lagging-leg turn-on (b, d, f) showing ZVS at these loads.

7. Experimental waveforms

Figure 13 gives the oscilloscope plot of the lagging-leg turn-off transient for a Mode 2 operation with and without the external inductor circuit. Current through the external inductor circuit is also recorded. As seen from the plots, there is a vast improvement in the turn-on transients by including the external inductor circuit.

Figure 14 shows the tank current and input voltage corresponding to 100%, 50% and 10% loads. Lagging-leg turn-on transients under the three load conditions indicate that ZVS is maintained throughout the operating range.

8. Conclusions

Soft switching is a desirable, if not an essential feature, in any power converter. This is more so for high-power switching converters where the power devices have to switch large currents at high-voltage levels. Soft switching is also needed for realizing high efficiency and low generated EMI specifications. The SRC is a preferred topology for high-power applications. Though

the SRC facilitates soft switching, the soft switching zones of operation are limited and depend on a number of parameters.

This paper addresses the design issues required for maintaining ZVS for the PM-SRC over the desired operating range. The different operating modes for the PM-SRC operating above resonance have been introduced and those modes which inherently facilitate ZVS have been identified. It is found that of the three modes of operation, only one facilitates natural ZVS. A modified PM-SRC circuit with a few extra passive components is introduced. The modification allows ZVS in all the modes of operation. Design relations obtained for ZVS are explained through a design example. The experimental results confirm that the modified circuit improves ZVS range. ZVS from 100% load to 60% load for the unmodified converter was improved to an extended range of 100% load to 10% load. Further, the ZVS feature enables stress-free operation in the otherwise undesired Mode 2 operation.

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