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A new sine wave inverter suitable for UPS application

P. MUKHERJEE, B. MAJUMDAR, S. K. BISWAS AND B. BASAK
Electrical Engineering Department, Jadavpur University, Calcutta 700 032. Bengal Engineering College, Howrah.

Abstract

A number of topologies are available for the inverter of Uninterrupted Power Supply (UPS). It is desirable that the inverter output should maintain a near-sinusoidal waveform. Of the various techniques developed, the high-frequency link Sine Pulse Width Modulation (SPWM) is most popular in compact, low-power category. In this paper, a new technique to generate low Total Harmonic Distortion (THD) sine wave form the low voltage battery bank is presented. A number of distinct advantages of this technique over existing also discussed.

Keywords: UPS, sine wave inverter, high frequency conversion.

Major Discipline: Power electronics circuits - Topology and control.

1. Introduction

A reliable, good quality power line is almost essential to modern sophisticated, precision apparatus, like computers, medical equipments, scientific equipments, on-line data processing instruments etc. In short, blackout, brownout, voltage spikes, harmonics and EMI are the major disturbances in power line, where blackout causes data loss, specially in case of computer under multi-user environment, which may cause an enormous problem in proper mounting of the file system as a normal shut-down procedure requires a certain period of time. Other problems in power line are often protected up to a certain degree by the suitable design, provided by the concerned manufacturer of the equipment. But a large and sustained voltage spike may cause a total hardware failure of the critical equipment. The only economic and effective method to solve all the above stated types of problems is to install an UPS. This leads to the increasing demand for compact, high performance and low cost UPS.

Static UPS including ON-LINE or OFF-LINE must have : a) battery charger b) battery bank (energy reservoir) and c) inverter, operated from the battery.

Different schemes are available for the inverter to produce a stable magnitude sinusoidal waveform with low total harmonic distortion (THD). Generally a THD <5% in a sinusoidal waveform is taken to be a good quality AC source. For low power UPS, since the battery bank voltage is low for economy, a step-up isolation transformer is necessary. If the step-up transformer is of power frequency, then the major cost, bulk and size will be contributed by the transformer and associated filter. So to fulfill the recent demand for compact,low-cost and energy efficient UPS, it is essential to replace 50/60 Hz transformer. This leads to the high frequency link type inverter system[1]. In this technique, the low volt-

age DC from the battery is firstly converted to an isolated high voltage DC with the help of a high frequency DC to DC converter. This high voltage DC is then converted to sinusoidal AC by SPWM inverter and LC filter.

An alternative approach using the high frequency link type technique to generate a low distortion step wave (which is very close to a sine wave) and then filter to get a very low THD sinusoidal output voltage, is being presented here.,

2. Stepped waveform generation technique

In the past, the stepped waveform[2] was synthesised by using multiple inverters in series, connected through power frequency(50/60 Hz) transformer. In the new technique presented here, power frequency output transformer are not used and the stepped waveform is generated by adding in series the pre-programmed PWM output of two inverters operating from two separate outputs from the step-up dc to dc converter. This technique can generate a stepped output voltage with low THD[3]. To obtain a low distortion sine wave from this stepped output voltage, only a very small filter is needed.

This technique has a number of distinct advantage over the conventional SPWM technique. Firstly, as the SPWM has to produce the commercial grade power, the devices used for this SPWM inverter must be capable of handling at least 2.5 times the output line voltage since the maximum fundamental output is 63.63%[4] of the dc bus with modulation index 0.9. But the scheme presented here, as the commercial voltage is produced from the two inverters in series the voltage handling capacity of the devices used in each inverter must be lower than the devices used for SPWM. Secondly, the control circuit of this present approach is less complicated than that of the SPWM technique since only one EPROM has been used here to produce the waveform pattern without the need for modulation and synchronisation which is essential for SPWM. Here, only the high dc bus is being controlled to achieve good regulation at the output of the filter *i.e.*, the final output of the total inverter. Thus, the harmonic content does not vary with load variation of the inverter or with the change in battery voltage . Finally, in case of the SPWM technique, it is possible to reduce the size of the output filter by increasing the switching frequency, but such a process increases the switching loss in the inverter, reducing the overall efficiency. In this present approach, the inverter switching frequency is not very high, improving the system efficiency.

The staircase generation stage consists of two pre-programmed PWM inverters, whose dc inputs are isolated and whose outputs are connected in series to produce a stepped waveform. It is obvious that the minimum THD is obtainable if the number of steps is increased. To obtain the best compromise between the number of inverters (*i.e*, the total number of switches used for inverter) and THD, a half-bridge and a full-bridge series combination has been selected. Two types of inverter switching schemes are possible, which are described in fig 1. The general rules for deciding the step heights for each case are described below.

For case 1,
Step height 1 = $V_2 - V_1$

For case 2,
Step height 1 = V_2

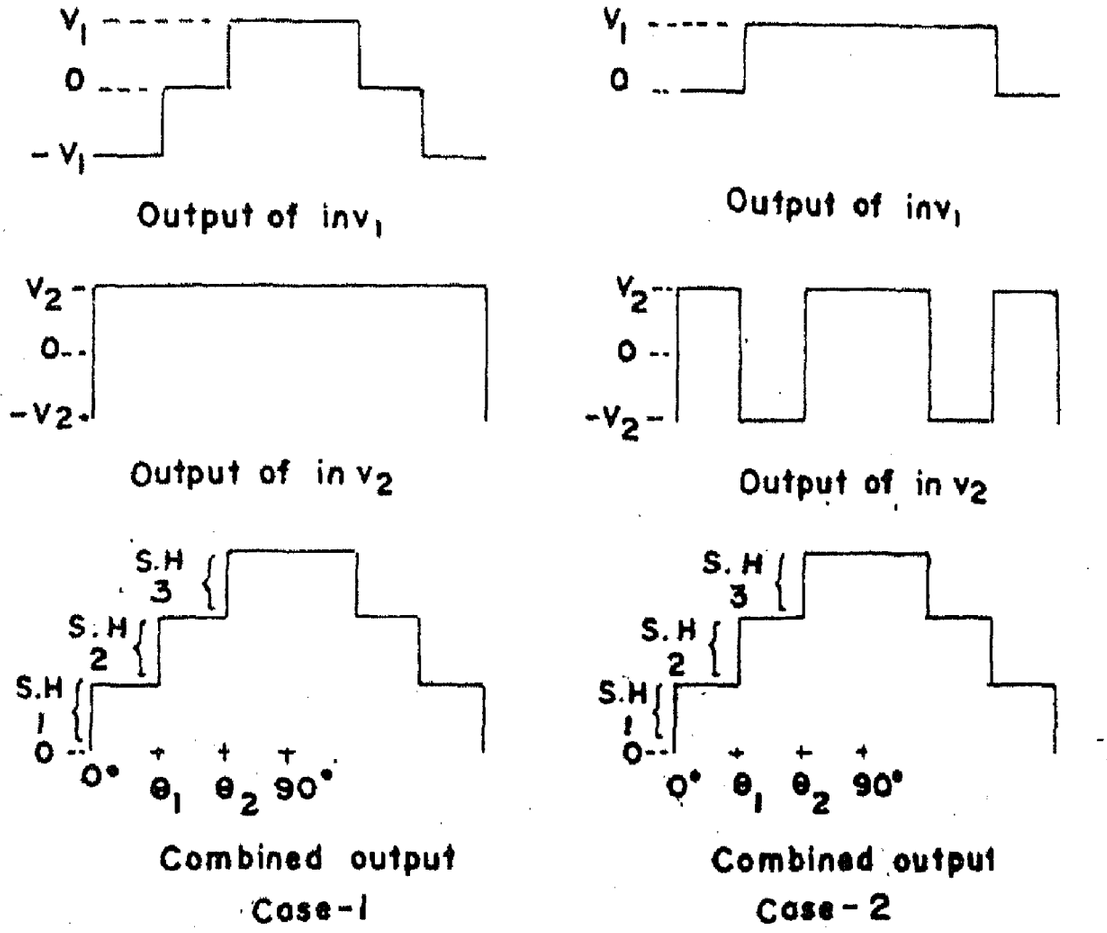

FIG. 1. Two types of inverter schemes.

Step height 2 = $V_2 - (V_2 - V_1) = V_1$
Step height 3 = $V_1 + V_2 - V_2 = V_1$
Where $V_2 > V_1$

1Step height 2 = $V_2 - 2V_2$
Step height 3 = $V_1 + V_2 - (V_1 - 2V_2) - V_2 = 2V_2$,
Where $V_1 > 2V_2$

So step height ratio = $(V_2 - V_1):V_1:V_1$. So step height ratio = $V_2: (V_1 - 2V_2):2V_2$

In general, the peak magnitude of the 'n'th harmonic of final output is given by[3]:

$a_n = 4*[E_1 \cos n\theta_1 + E_2 \cos n\theta_2 + \ldots + Ek \cos n\theta k]/n\pi$....(1) where Ek is the step height at position θk.

In all the above equations, the value of n exists only for odd numbers due to waveform symmetry.

Since there is no simple way to compute all the possibilities, only an iterative process has been used.

Out of several combinations possible, a few has been listed, requiring minimum filter.

Percentage THD is given by:

$$\text{percent } THD = \frac{\sqrt{\sum_{n=2}^{\alpha}(a_n)^2}}{a_1} \tag{2}$$

Studying the above list, it is found that 1st case is the only case where the minimum filter is required to minimize all the harmonics below 3%, such that the THD can be ensured to be below 5%.

3. Filter Calculation

For the simple low pass filter, if the input voltage of 'n'th harmonic be V_{in} and the output voltage be V_{on} then it is known that,,

$$V_{on} = \frac{(1/jn\omega C)*V_{in}}{(1/jn\omega C)+jn\omega L}$$

$$= \frac{V_{in}}{1-n^2\omega^2 LC}$$

$$i.e.,\ LC = \frac{1}{n^2\omega^2}\left[\frac{V_{in}}{V_{on}}+1\right] \tag{3}$$

In the filter circuit the voltage drop across the filter inductor, is given by,

$$V_L = I\omega_1 L \tag{4}$$

Where ω_1 is the fundamental output frequency and as maximum 10% voltage drop is permissible across the filter inductor, the value of the filter inductor was found 73mH.,

The current through the filter capacitor is given by,

$$I_c = \omega_1 V_0 C \tag{5},$$

Using the above formula, it is found that the values of L and C is 73 mH and 2.6 7 μF for 230 Volt / 1Amp inverter.

4. System configuration

The complete inverter system, as depicted in fig.2 uses two inverters in series, and has three basic stages (1) a step-up dc to dc converter with isolation, producing the isolated voltages V_1 & V_2 and (2) a pair of inverter stages consisting of one full bridge and one half bridge, generating the stepped output waveform and (3) the LC filter, producing the final sinusoidal output voltage.

The dc to dc converter, switching at a frequency of 50 KHz, configured as a push-pull circuit due to lower cost in low voltage application. The two ac isolated output are rectified by individual bridge rectifier using ultra fast recovery diodes. The two rectified dc are filtered with LC filter where the three dc chokes are coupled together through a single

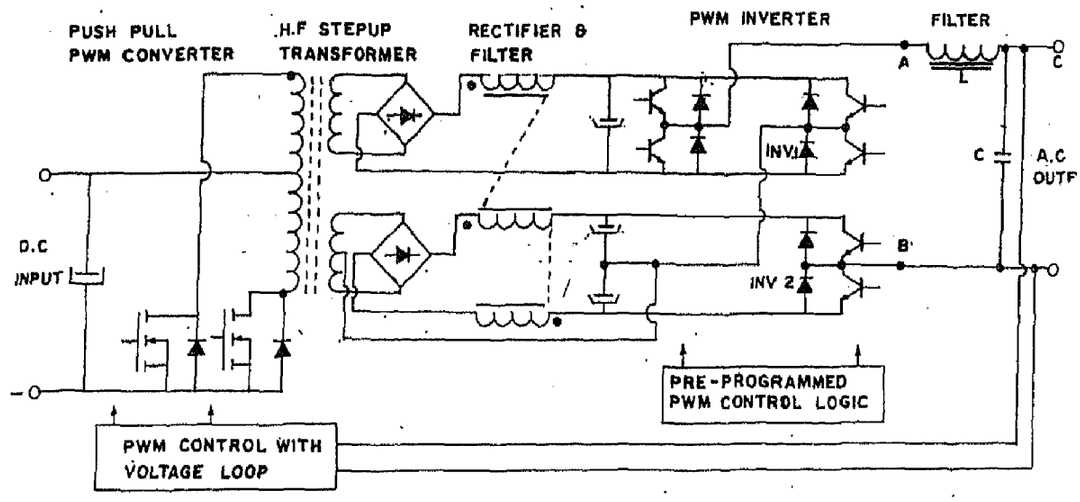

FIG. 2. The complete inverter system.

magnetic core to maintain reasonable good regulation of the output voltages while the chokes also serve to smoothen the voltage ripple[5].

The inverter scheme presented here is an unidirectional system. Hence, when this inverter is used in a complete UPS system, a separate battery charger is necessary. As this inverter scheme has no relation with the charger scheme, any suitable type of battery charger can be used, *i.e.*, either a phase controlled battery charger or SMPS based battery charger.

The transient response of this inverter is very good as the inverter output voltage is controlled from the dc to dc converter and not by the inverter itself. Since the switching frequency of the dc to dc converter is high (here a 50KHz switching is used), so the voltage correcting action is also very fast. Hence, the load transient on the inverter or any transients appearing on the input dc voltage creates a marginal effect on the r.m.s. value of the output voltage or on the waveform pattern.

In an actual application, the inverter output must be protected against short circuit. The short-circuit protection of the inverter is in no way related with the basic scheme of the inverter. This can be excellently achieved with the help of standard intelligent base drive circuit described extensively in literature[6]. An overload detection circuit can be however incorporated using a current sensing transformer to sense the inverter output current and taking action to shut down the dc to dc converter used to generate the two separate regulated high DC voltages. But this process does not permit the system to withstand short circuit due to stored energy existing in the dc bus capacitor of the converters.

5. Simulation and optimisation

Although it was found that the filter size is less in the first case of the table I, but harmonic analysis with PSPICE simulation does not tally with the theoretical calculation.

Table I
Harmonic contents (theoritical) of step wave for different step angles

		Harmonics present in % of fundamental					
Step angles	Step height ratio	3rd	5th	7th	9th	11th	13th
0°, 24°, 51°	1:2.2:2	0.79	2.90	2.83	2.84	2.34	6.51
0°, 22°, 50°	1:2.5:2	2.07	2.34	2.24	3.32	4.24	3.95
0°, 25°, 53°	1:2:2	2.89	1.61	3.46	3.65	0.60	8.32
0°, 23°, 50°	1:2.3:2	0.71	2.98	2.58	2.64	3.40	4.88
0°, 24°, 54°	1:2.2:2	1.76	0.48	2.56	5.18	0.89	8.03

Table II.
Comparison of theoretical and PSPICE simulated harmonic contents of output at different stages

			Harmonics present in % of fundamental		
Step angles	Step height ratio	Order of harmonic	Theoretical value	Simulated value (before filter)	Simulated value (after filter)
0°, 24°, 51°	1:2.2:2	3rd	0.79	1.12	1.06
		5th	2.90	1.65	4.32
		7th	2.83	3.11	3.64
		9th	2.84	4.29	1.76
		THD	5.01	5.66	6.01
0°, 24°, 54°	1:2.2:2	3rd	1.76	1.40	2.45
		5th	0.48	0.75	0.73
		7th	2.56	3.29	1.97
		9th	5.18	5.53	1.99
		THD	6.07	6.64	3.80

This is due to the fact that in the theoretical calculation, the finite switching time was not taken into account. So a further optimisation was needed. Though the last example of the table I gives an unimpressive look from the harmonic content aspect, this gives a better result in PSPICE simulation with minimum filter requirement of 4.47m1f capacitor along with the inductor value of 73mH, using eqn.(3). This may be further clear from the table II, given below.

From the above table-II, it was found that the finite switching creates a difference from the theoretical value of the harmonic content. ,

From the filter calculation it was found that the simple LC filter cuts down the higher order harmonic at the cost of increasing the lower order harmonic content. Theoretically it also tallies with the equation (3). So a further iteration was required as the PSPICE is not an interactive software. From the table-II, it is clear that the step wave which contains very low lower order harmonic content gives a better results as in that case the filter cannot increase the lower order harmonic content to a significant level, which ensures that the THD will be small after the filter. PSPICE simulated curves of step-wave and filtered output corresponding to step angles 0°, 24°, 54° at a step height ratio of 1:2.2:2 has been presented in fig. (3) and fig. (4) respectively.

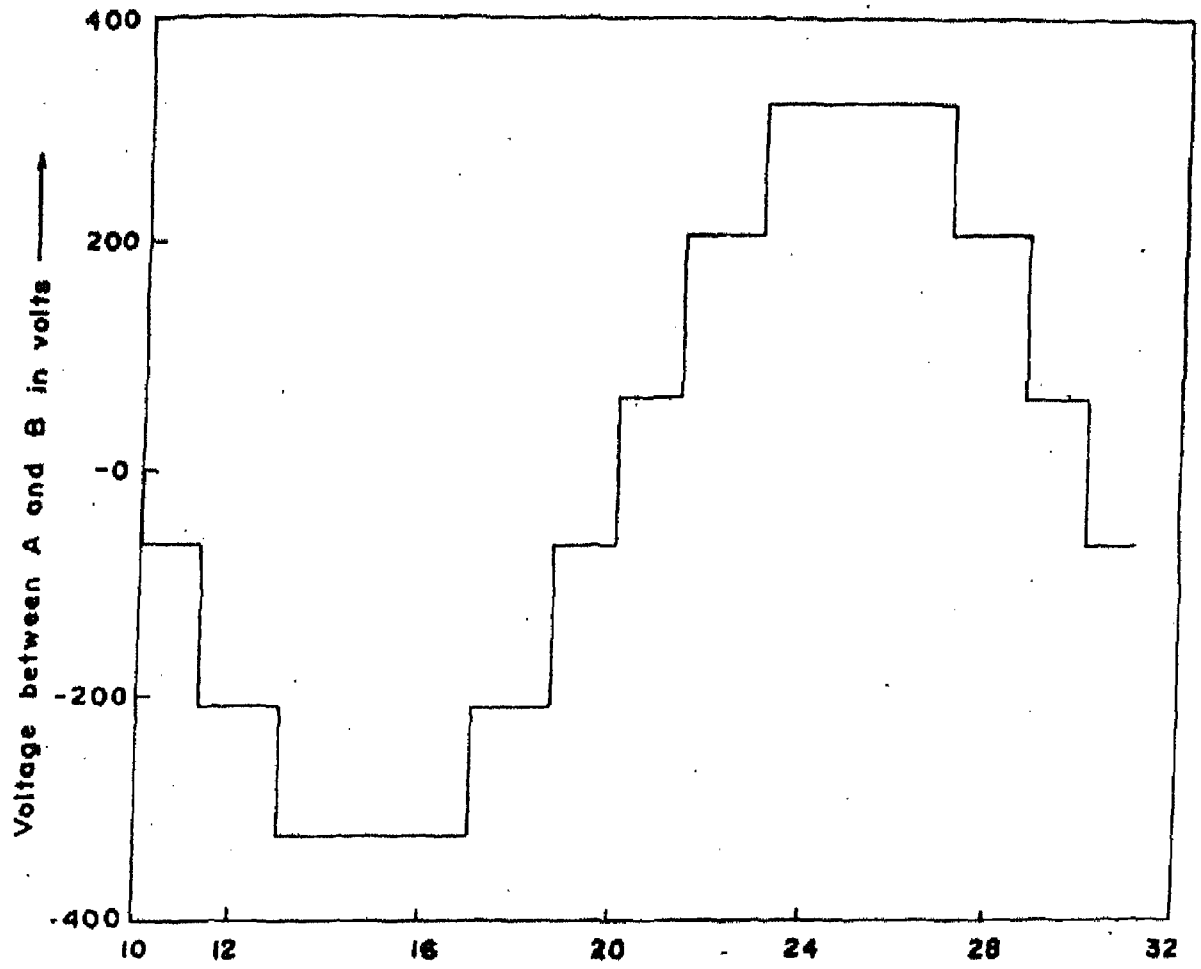

FIG. 3. PSPICE simulated curve of step-wave output for step angles of 0°, 24°, 54° at a step ratio of 1:2. 2:2.

As it is impossible to calculate all possible step combinations, only a few has been studied and the best out of those had been listed here.

6. Experimental results

A prototype inverter based on step angles 0°, 24°, 54° at a step height ratio 1:2.2:2 has been made and tested in the laboratory. It is rated 230 VA at 230 Volts, 50Hz. The push-pull converter was designed to operate at 50 KHz using parallel-connected MOSFET's. The ferrite core transformer output windings were in the ratio of 1:2.1. The output of the inverter was directly loaded with either a 200 Watt lamp or to a computer. Fig. 5 shows the plot of the step wave output (*i.e.*, before filter circuit at the point between A and B in fig 2.) and the fig. 6 shows the plot of the sine wave output (*i.e.*, after filter circuit at the point between C and B in fig 2.) with the rated load. The measured THD at the rated load is only 4.79%.

7. Comparison between spwm and new technique

In case of conventional SPWM with the high frequency link technique is considered here. In this case the sine wave modulation index is fixed where the output ac voltage may be controlled by regulating the high voltage dc bus obtained from the dc to dc converter. In

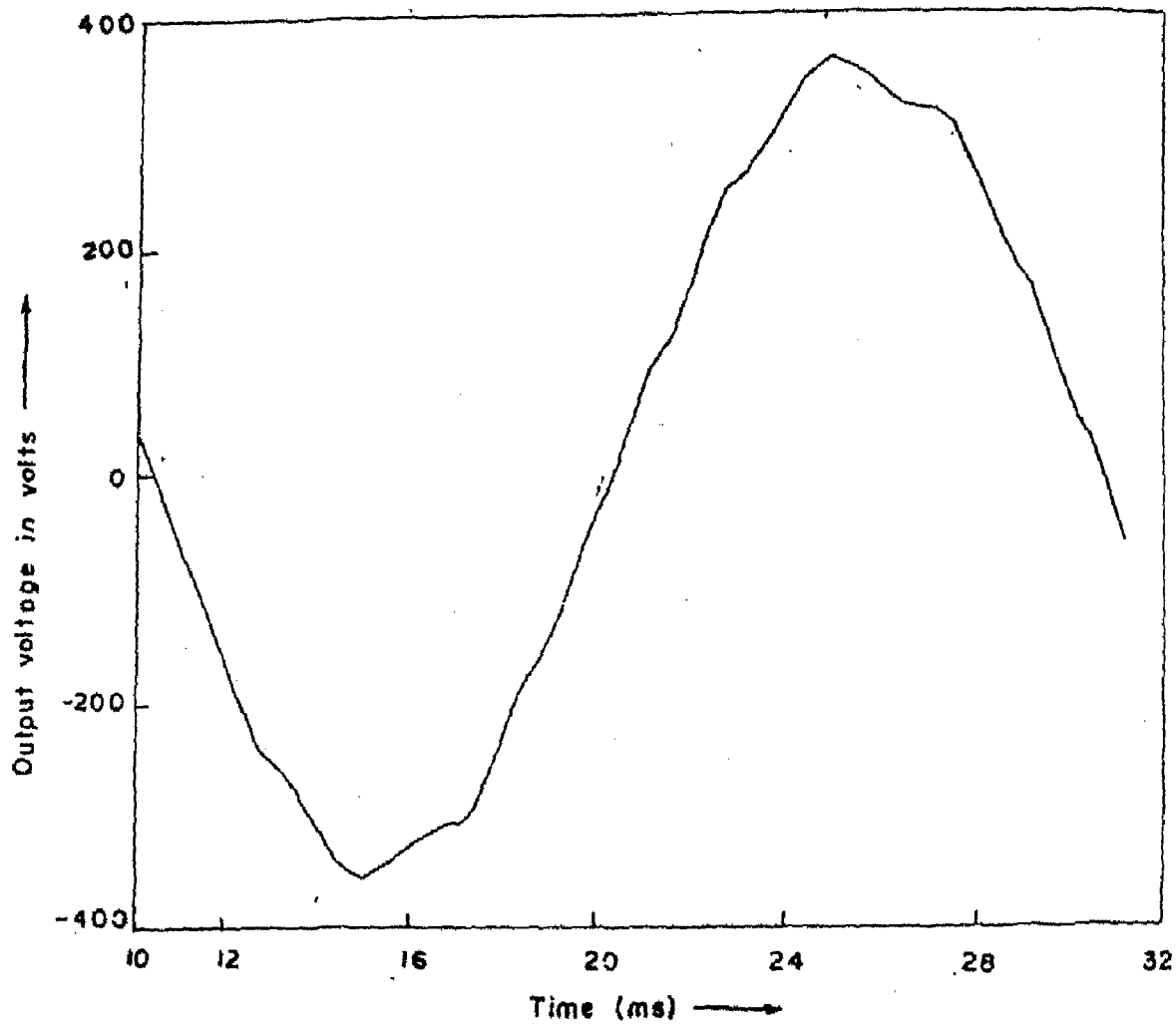

FIG. 4. PSPICE simulated curve of filtered output for step angles of 0°, 24°, 54° at a step ratio of 1:2. 2:2.

this mode of operation the stress over the switches is minimum if the modulation index be 0.9. In a SPWM where zero of sine wave coinciding with zero of the triangle and the number of triangles per cycles being 6 is considered here. Thus, for a bridge inverter there will appear 5 pulse per half cycle, which is comparable with the new technique that uses only five switchings per half cycle. As the harmonic content does not vary whether the triangle is synchronised with zero of sine or with 90° of the sine, the dominant 9th harmonic is, 19.64%[4]. From the filter circuit calculation given above, it is found that the required filter capacitor is 10 μf to reduce the THD below 5% with the same filter inductor 73 mH and the filter capacitor current (no-load current)is about 70%. Theoretically, the filter values are calculated to reduce the 9th harmonic to 4%, assuming the THD will be below 5% limit. In comparison, the new stepped wave technique demands only 4.4 μf filter capacitor with the same inductor, reducing the no-load current to 30%.

8. Conclusion

This paper presents a new approach to the generation of a low distortion sine wave output which is useful for UPS application. As the output voltage is obtained from two inverters

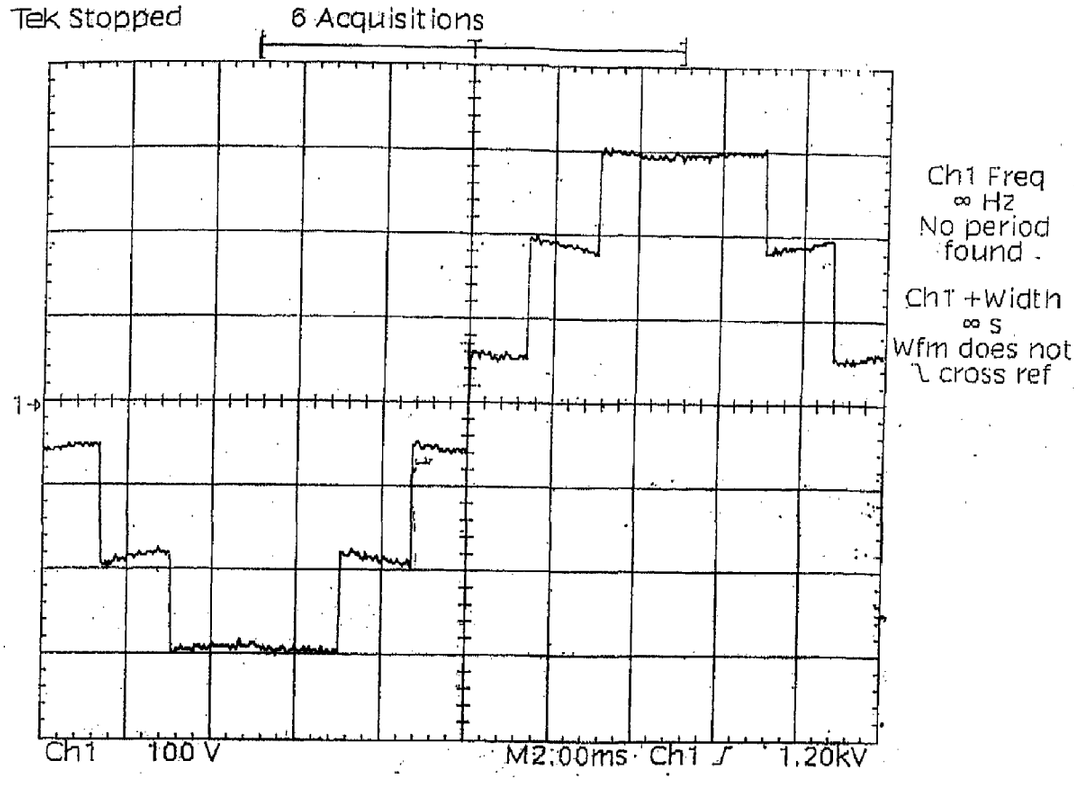

FIG. 5. A plot of the setp-wave output.

in series, and as the switching frequency is low, so low cost, bipolar transistors were used here. Also for this application, the corresponding bridge rectifiers and the filter condensers of the DC to DC converter were of relatively lower voltage capacity type, reducing the cost of the inverter. The output THD is greater than that of simulated value because of two main reasons, firstly the PSPICE simulation was done with the concept of ideal dc bus voltages but in practice it is found that the dc bus voltages contain finite ripple, which can be seen in fig. 5. Secondly an additional delay was given to the rising edge of the drive to each switch to protect against shoot-through, which was not considered in the PSPICE simulation. As the filter capacitor takes only a small percentage of the full load current, it is healthy for battery bank at light load and a longer backup time can be obtained from the same battery bank with respect to the SPWM in same load condition, considering system losses. Though the filter is simple and small in size, a further small filter can be used by further optimising the step angles and the dc bus voltages ratio with the same inverter configuration.

9. Acknowledgements

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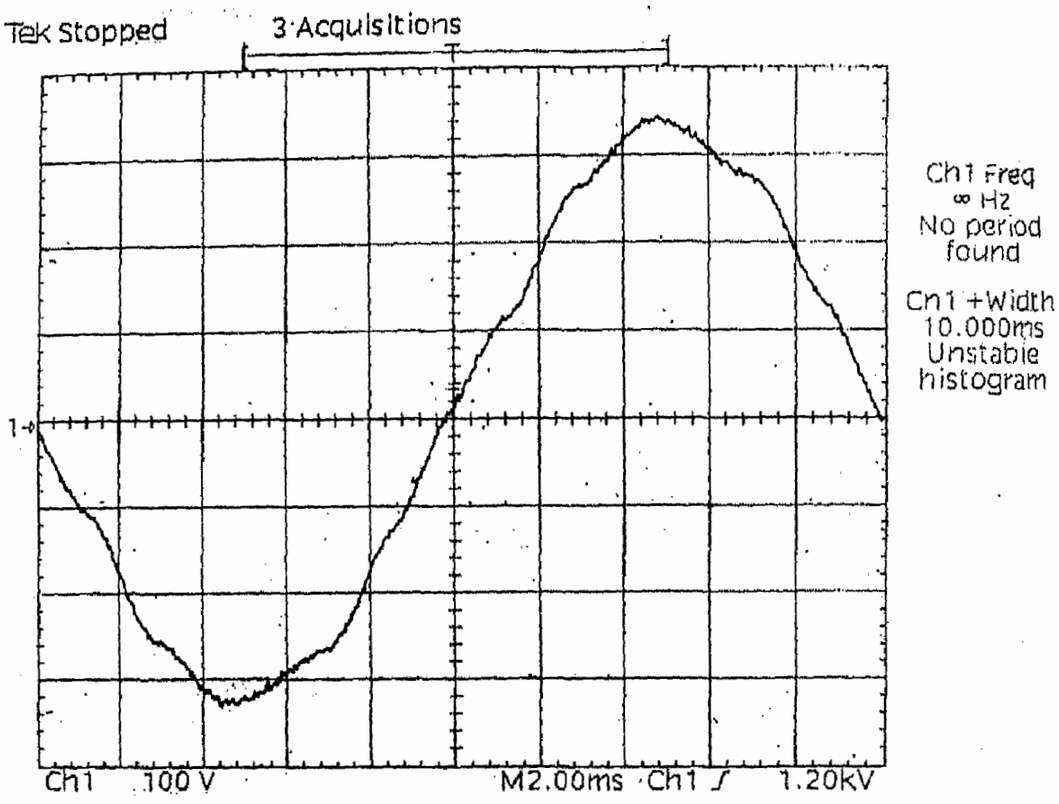

FIG. 6. A plot of the sine-wave output.

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